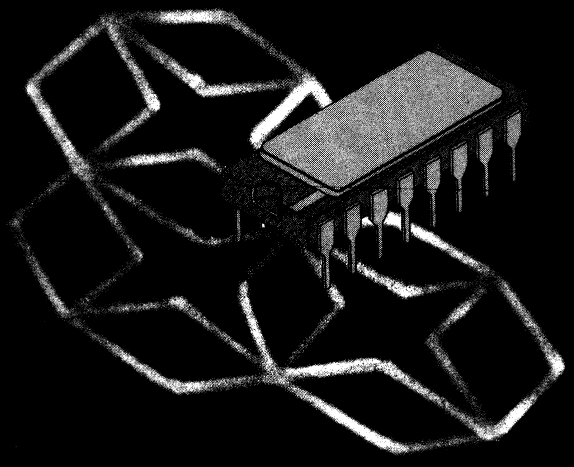

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M. Dekkers

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CHAPTER I INTRODUCTION

1.1 General

This manual establishes the basic philosophies and procedures of quality programs implemented by Samsung Semiconductor and Telecommunication Ltd. A clear focus on the critical nature of reliability and quality makes Samsung a leader in semiconductor product assurance.

Samsung has been providing a wide variety of semiconductor products to the world for many years. Extensive inroads and insights have been used to create methods which most effectively result in reliable products. As a developer and user of Statistical Process Control curricula, Samsung pays strict attention to manufacturing reproducibility. Long ago realizing the key to enhanced reliability was process control, stringent statistical analysis has been instituted by Samsung for many years.

Fully described within this manual are the quality assurance procedures which Samsung carries out to guarantee the integrity of its products. Items detailed include general standards, tests performed and test results, process and document control, assurance operations, customer support, and failure analysis methodologies.

1.2 Policy

Samsung's semiconductor division management philosophy is to manufacture a product commensurate with corporate policy and customer contract requirements. Samsung sets its standards to exceed those of the most rigorous consumers, such that any customer will receive only completely qualified product.

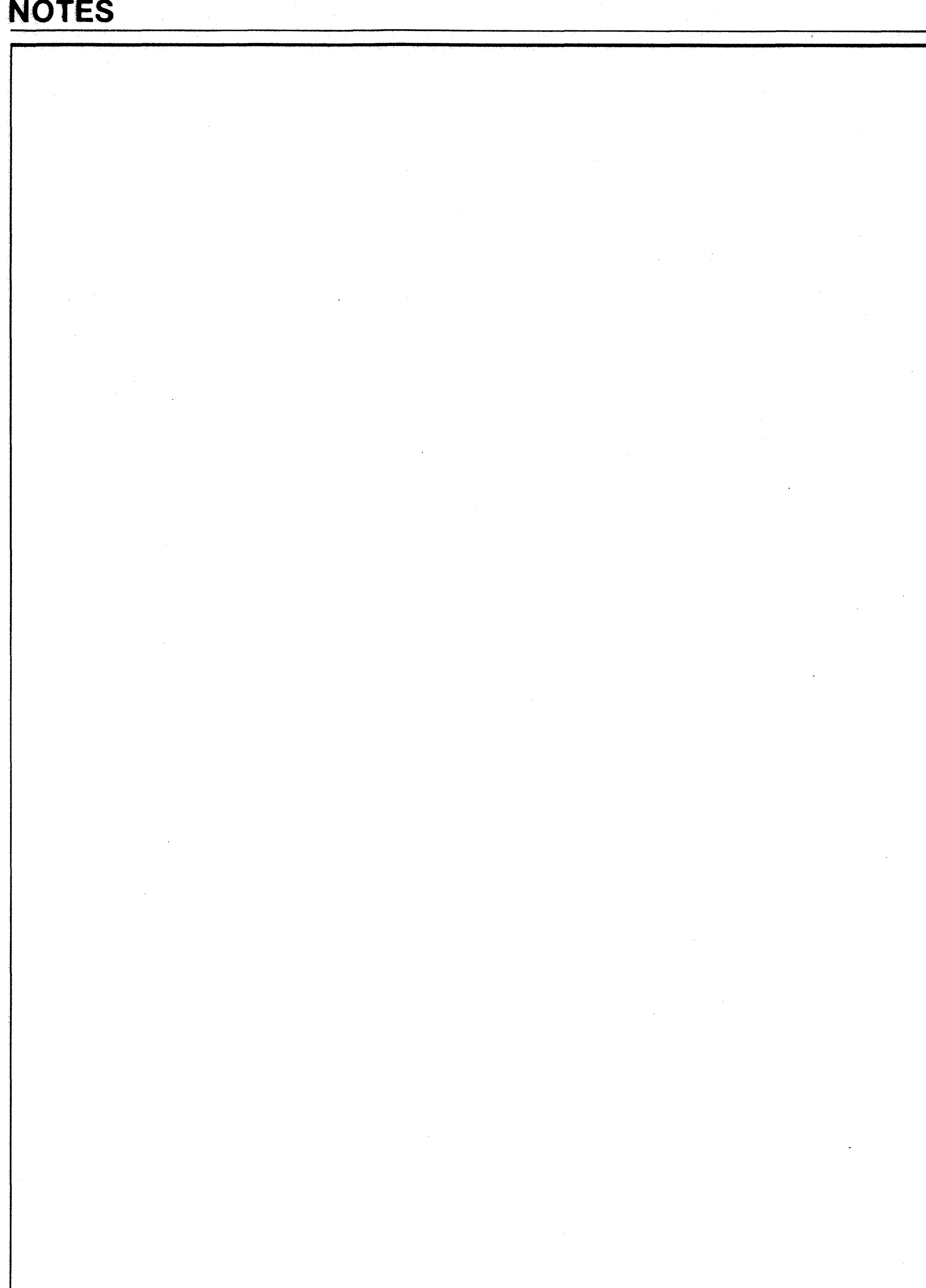
It is the responsibility of the reliability and quality department to assure that these requirements are met.

1.3 Scope

The policies discussed above have been established to provide a quality program in the areas of design, development, production, inspection, and test for semiconductor products.

In the event of any inconsistency between this document and specific contractural requirements and schedules, the contract requirements and schedules will take precedence.

NOTES



CHAPTER II QUALITY MANAGEMENT and ORGANIZATION

2.1 General

Samsung has adopted a TOTAL QUALITY CONTROL approach, which means that everybody in the company contributes to quality improvement. Such an approach can solve quality problems at the stage where they arise, so that latent failures are not carried over to the next stage, or to finished goods. TOTAL QUALITY CONTROL assures the prevention of quality problems, rather than simply eliminating defective finished products. Naturally the customer benefits from the approach, as it quarantees very strong quality and reliability. As a consequence, costs to the customer for their finished products are reduced.

2.2 Policy

It is the company's policy that all products shall be efficiently and economically manufactured in compliance with uniformly high standards of quality. The quality department has full responsibility for establishing and implementing any procedures necessary to ensure this policy.

The organization of the company ensures that the quality function will at all times have the authority to carry out this policy. As Fig. 1 demonstrates, quality assurance reports directly to the presidential level, while quality control also reports to an upper management level.

2.3 Scope

The quality organization sets quality control and reliability targets for all products, defines procedures and the specification system, and regularly audits their implementation. Application is to all manufacturing stages, and includes heavy interfacing with development and production personnel. The quality group is also responsible for the evaluation of new processes, the development of advanced failure analysis techniques, reliability prediction, and advanced reliability studies utilizing novel techniques. When a customer requires additional quality controls or special reliability procedures for product, the quality department ensures compliance to the particular specifications.

2.4 Quality Department Organization

Figure 1 delineates the differing sections and their functions within the quality organization. Both quality control and quality assurance are detailed.

2.5 Quality and Reliability Function Procedure

From development to customer after-sales service, the product assurance system is outlined in Figure 2. Qualification testing for new products, significance testing for engineering changes, in-process quality controls, batch acceptance testing, periodical reliability testing, and customer service are all performed under a unified system.

2.6 Education and Training

Management at Samsung has always given top priority to quality. For this reason, the quality department has organized a quality training program. Training seminars, sometimes with external consultant's support, are run at all levels. This starts from upper management, and includes engineers, quality personnel, production supervisors, and workers. The objective of the training seminars is to improve quality and reliability, to reduce costs by eliminating rejects, to promote greater awareness of the importance of quality, and to encourage participation in the solution of quality-related problems.

QUALITY MANAGEMENT AND ORGANIZATION

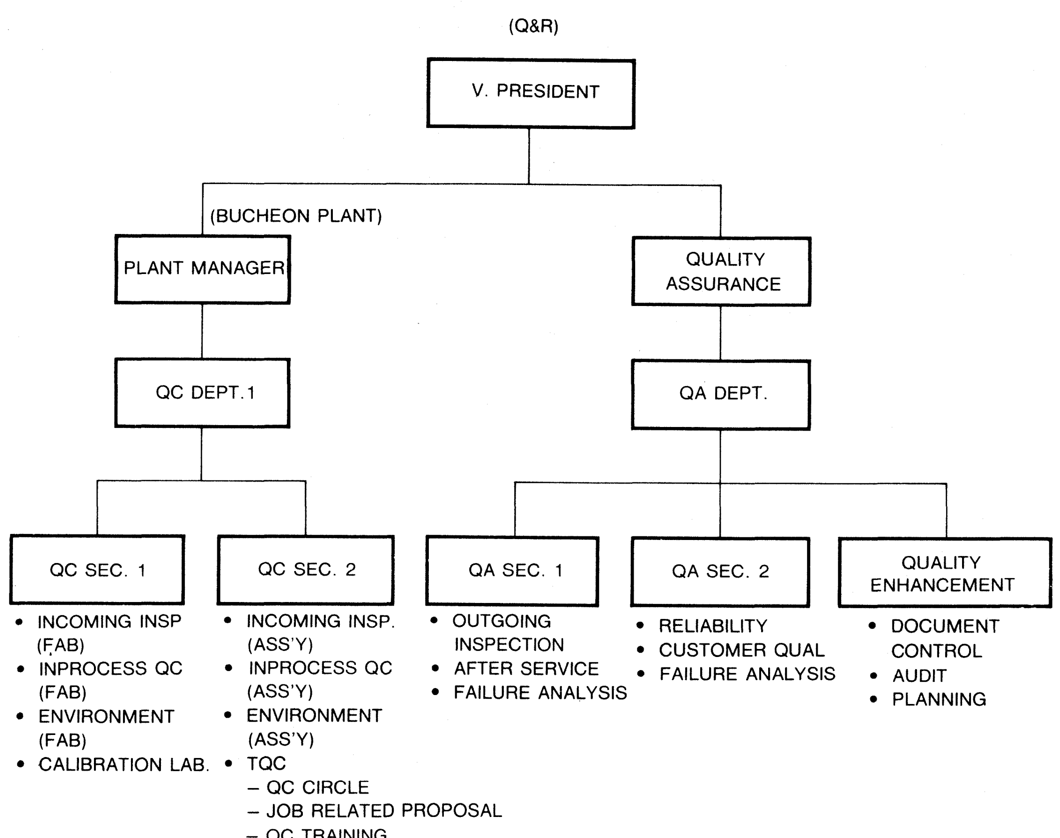


Fig. 1. Quality control organization chart

STEP | SALES | APPLI-CATION | DESIGN | PROCESS ENG'S | QC/QA | PRODUCTION | PRODUCTION CONTROL

PLANNING

MARKET SURVEY

SPEC. REVIEW

COUNCIL FOR DEVELOPMENT

DESIGN & TRIAL MFG

DESIGN

DESIGN REVIEW

QUALIFICATION OF RAW MATERIAL

TRIAL MFG (ENGINEERING RUNS)

EVALUATION & QUALIFICATION

PRE-PRODUCTION

STANDARDIZATION

APPROVAL

PRE PRODUC-TION (P.P)

QUALIFICATION

MASS PRODUCTION

INCOMING INSP

PROCESS CONTROL

MASS PRODUCTION

PROCESS MONITOR

RELIABILITY TEST

LOT ACCEPTANCE TEST

FAILURE ANALYSIS

SHIPPING

MARKET

CLAIM

INITIATE CORRECTIVE ACTION

CUSTOMER

Fig. 2. Quality and reliability function procedures

NOTES

CHAPTER III PROCESS CONTROL PROGRAM

3.1 Process Control Policy

The policy of the company on process control is as detailed below.

3.1.1. Any operation, test, or measurement used in manufacturing must be formally specified.
The approval of a quality engineer is required for all specifications relating to purchased items, along with all specifications relating to the manufacture and testing of standard and custom products.

3.1.2 Purchased materials and piece parts must be ordered to a formal specification from an approved supplier. Purchased items must be checked against the purchase specification and accepted by the quality department before being used.

3.1.3 The manufacturing department is responsible for performing operations and processes in accordance with specifications, and for the manufacturing quality of the product. The quality function, in particular quality control, is required to ensure that specified methods are used, and that specified quality standards are maintained by the methods listed in the following sections.

3.2 Process Control Methods

The quality control department assures compliance with the above policy by:

3.2.1. Auditing processing methods.
3.2.2 Performing in-process and finished product monitoring.
3.2.3 Providing information for, and assuring completion of, corrective action.
3.2.4 Providing criteria for (and means of) identifying acceptable and defective product.
3.2.5 Conducting monitor control in conformity with processing and fabrication specifications.

3.3 Data Reporting

3.3.1 Process control data is recorded on an attribute basis or form as required, with control charts maintained on a regular basis. This data is reviewed periodically and serves as the basis for judging the acceptability of specific processes.

3.3.2 Inspection reporting
The result of each inspection, confirmed by operator and inspector, is recorded on a quality control form and/or computer. Defective work is reported immediately to production supervisors, in major cases using an in-process rejection form designed to convey the relevant data. A copy of every inspection result is submitted to the chief inspector.

3.3.3 Summaries of results
The results of inspection, normally summarized on a weekly basis, are presented on summary forms. The results may be compared with historical data, so that the trends for overall quality can be seen. Summary data from the various process control operations are relayed to cognizant line, engineering, and management personnel in real time. Thus, if appropriate, corrective actions can be taken immediately.

3.4 Corrective Action

3.4.1 General
Checks are made throughout the receiving, manufacturing and test operations to identify existing or potential deficiencies in company products. When these checks indicate conditions which may result in substandard or defective material, preventative actions are undertaken. In addition, customer feedback data, along with requests for failure analysis and corrective action, are a part of the actual checking system.

3.4.2 Corrective action procedure
There are three formal levels of corrective action which may be taken under the corrective action procedure shown in Fig. 3.

PROCESS CONTROL PROGRAM

1) Following the failure of an in-line or batch acceptance sample at a quality control or production inspection, action is taken by production to screen, rework, or scrap the defective lot. To prevent a re-occurence of the fault, any necessary action is undertaken.
2) If action at the first level is ineffective, or if the fault persists, a quality engineer describes the status of the failure on appropriate documentation. This is then directed to the production engineer in charge and to the manager of the area concerned. The engineer is required to take corrective action immediately. The quality control engineer monitors the adequacy of this action, to ensure the problem is being addressed properly. If corrective action is neither taken nor effective, the next higher level of management is involved in the matter until the problem in question is solved.
3) If quality is directly affected, a work stoppage may be enforced to prevent further production of defective material.

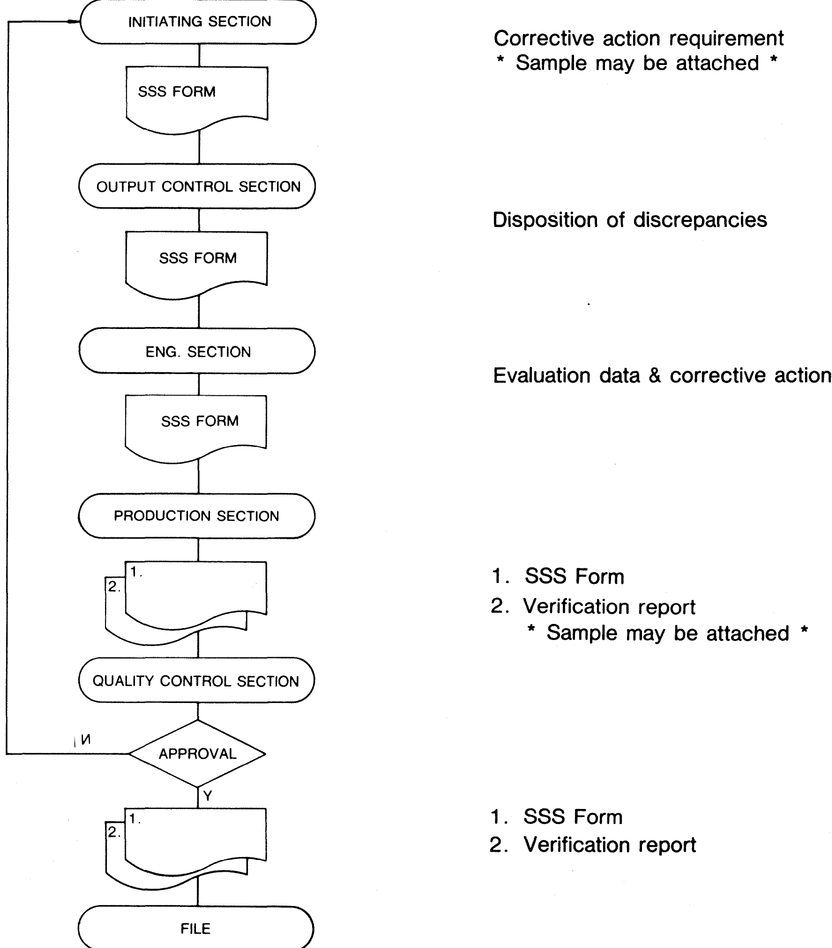


Fig. 3. Corrective action procedure

3.5 General Process Control

Samsung's general process flow is shown in Fig 4.
This illustration contains the standard process flow from incoming parts & materials to customer shipment.

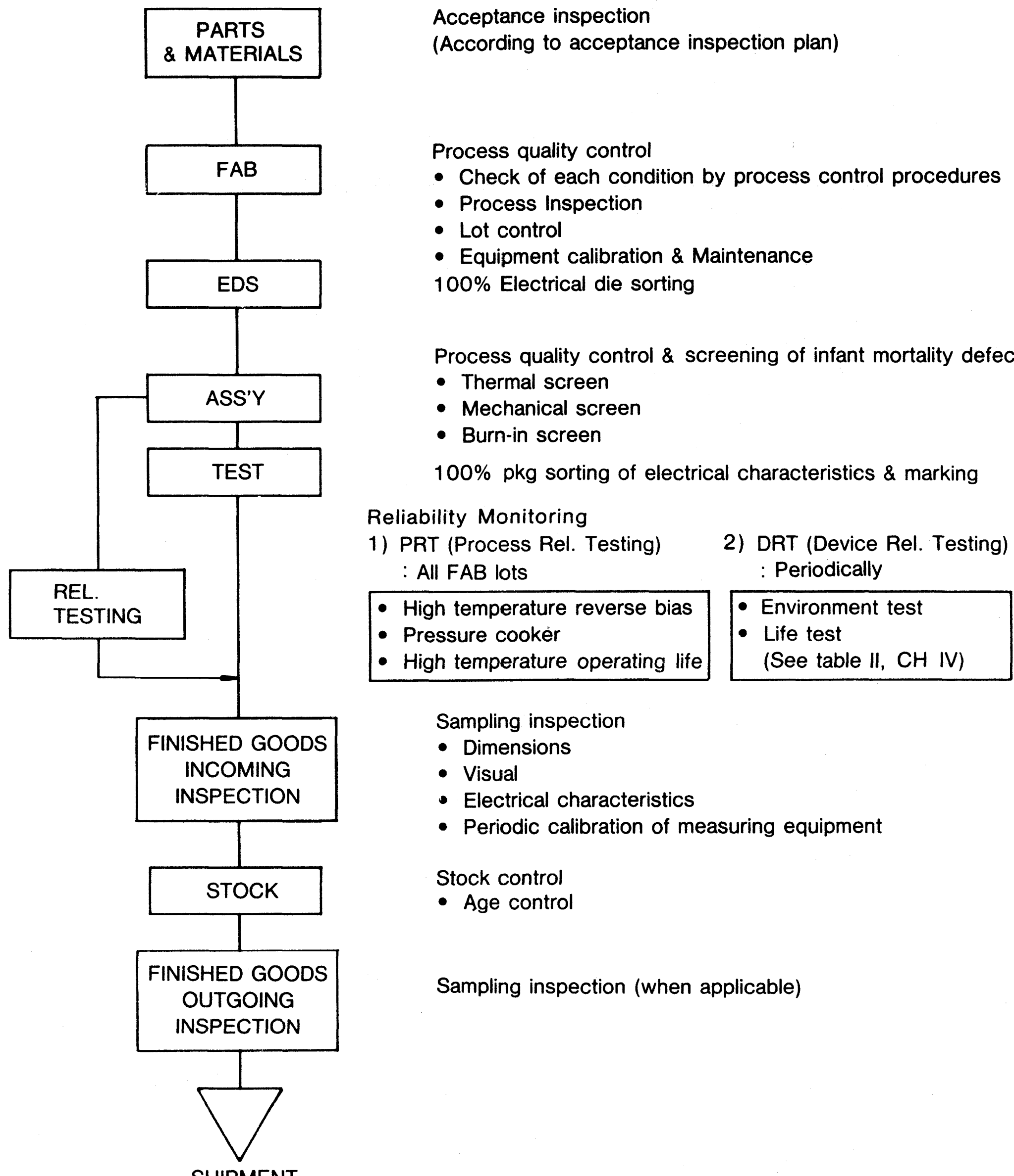


Fig. 4. General process flow chart

3.6 Wafer Fabrication (Raw material incoming inspection)

Samsung itself manufactures few materials used for wafer fabrication. Silicon, chemicals, and other materials are all purchased from Samsung-qualified and-approved vendors.
To ensure that only materials of the highest quality are used. Samsung has an evaluation system (program) for vendor quality improvement.
This evalution system operates under the following policies:

1. Establish technical relationships with Samsung's selected vendors to mutually improve the entire technology.
2. Improve product quality through mutual interaction to achieve low defect levels. In this way, Samsung incoming inspection becomes a data-gathering activity.
   This program is manifested in a vendor quality evaluation report, in which vendors measure product quality to Samsung specifications, and Samsung accepts product based on vendor-supplied data.
3. Base purchase allocations are made on quantitative vendor comparisons, where quality, delivery, total cost, and vendor responsiveness to Samsung are considered in determining each vendor's ranking and rating.

3.6.1. Wafer inspection

Inspection procedures are based on three categories:

1. Visual inspection
2. Dimensional inspection
3. Material property measurement

During inspection, discrepant lots are occasionally encountered. The disposition of discrepant material is to normally return it to the vendor. However, if the material is deemed as suitable for use, there are many possible resultant actions:

1. 100% screen the incoming material to physically remove defective items.
2. Modify the Samsung specification if it is discovered through reject analysis the specification is improper.
3. QC actions are all documented and have lead to vendor or internal corrective actions.

Table I lists the silicon wafer inspection techniques used at Samsung.

(Table I) Silicon Wafer Inspection techniques

Purpose	Instruments	Sample
• Structural — Crystallographic Defect	— Secco Etch — Sirtl Etch (Microscope)	All Lots (Small Sample)
• Electrical — Resistivity — Conductivity type	 — Kokusai VR-30A (4 Point Probe) — Tencor Sonogage — ASM AFPP — Mercury Probe (811) (MDC CSM System) — Tencor Ten-Type	All Lots
• Dimensional — Thickness — Diameter — Orientation — Flatness (TIR)	— Non-Contact Thickness Gage (ADE6034) — EPI-Layer Thickness Gauge (Digilab FTG-12) — Qualimatic S-100 — Flatness Measuring System (Siltec)	All Lots
• Visual — Surface Quality — Cleanliness	— Automatic wafer Inspection System (Aeronca WIS-150) — Unaided Eye	 All Lots All Lots

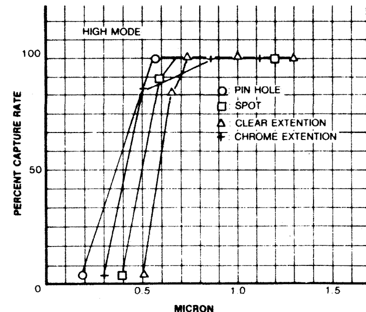
3.6.2 Mask Inspection

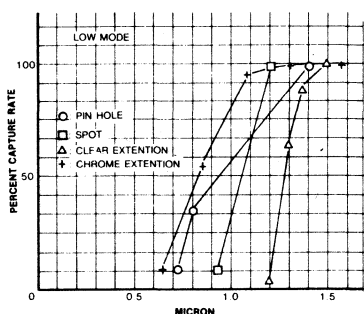
Mask parameters and tolerances are established by design and development engineers. Samsung utilizes state-of-the-art automatic inspection instrumentation with guaranteed repeatability. Recent results demonstrate nearly zero defects greater than 0.7um in the case of the incoming masks. Samsung reinspects photoplate masks after every 10 times of use as part of it's preventative maintenance procedures. Table II lists the mask inspection technology currently used as Samsung.

(Table II) Mask Inspection Technology

Purpose	Instrument	Sample	Criteria
• Defect Detection – Pin Hole & Clear-Extension – Opaque Projection & Spots – Scratch/Partice/Stain – Substrate Crack/Glass-Chip – Other	NJS 5MD – 44 (Auto Mask Inspection System)	All Masks	≤ 1.5 um Defects ≤ 0.124 ea/cm Defect Density
• Registration – Run–Out (X-Y Coordinate) – Orthogonality – Drop-in Accuracy – Die Fit/Rotation	MVG 7×7 Comparator	20% All New Masks 100%	~ 0.5 um Defects
• Critical Dimension	MPV–CD 1,2 Automatic Line Width Measuring System	All Masks	Purchasing Spec.

* Mask Defect Capture Rate (Graph)





3.6.3 Chemical inspection

Examples of relevant chemicals are photo resists, developers, solvents, acids, and dopants. Chemical composition and related characteristics aren't normally subject to a physical incoming inspection. Samsung receives the certification card and/or outgoing inspection result of a particular vendor and judges for proper quality. Examination consists of, but is not limited to: proper composition, proper concentration, and expiration date.

The chemical container, which must be free from any contamination, must be quality assured at incoming inspection. Naturally materials and their properties are monitored during production to assure that quality is maintained.

3.6.4 Wafer Fabrication

3.6.4.1 Process control

Quality programs utilize the following methods of control to achieve previously stated objectives: process audits, environmental monitors, lot acceptance inspections, and process integrity audits. A general wafer fabrication flow is shown in Fig. 6.

3.6.4.2 Definitions

Essential components of the quality control program are defined as follows:

1) Process audit –performed quarterly on all operations critical to product quality and reliability.
2) Environment monitor – monitors concerning the process environment. Examples include water purity, temperature, humidity and particle counts.
3) Process monitor – periodic inspections at designated process steps to verify manufacturing inspections and maintenance of process averages. These inspections provide both attribute and variable data.
4) Lot acceptance – lot by lot sampling. This sampling method is reserved for those operations deemed as critical and, as such, require special attention.

3.6.4.3 Environmental monitor

(Table III Environment Monitoring Item)

Process	Control item	Spec. Limit	Insp. Frequency
Clean room	• Temperature • Humidity • Particle (≥0.3um) • Air velocity	• Individual spec. " " "	1 HR 1 HR 1 HR 1 HR
D.I Water	• Particle – Main – Using point	 • < 4 ea / 1 ml • < 7 ea / 1 ml	 1 HR
	• Bacteria – Main – Using point	 • 50 Colonies/100ml (0.45um)	 Weekly Monthly
	• Resistivity – Main – Using point	 • ≥ 16 Mohm-cm • ≥ 14 Mohm-cm	 1 HR 24 HR
	• Silica count	• < 20 PPB	24 HR

* Instruments
- FMS (Facility monitoring system) – HIAC/ROYCO
- CPM (Central particle monitoring system) – Dan Scientific
- Liquid dust counter
- Filtration system for bacterial check
- Air particle counter
- Air velocity meter

3.6.4.4 Process controls and monitors

A Basic listing of process controls and monitors is presented in Table IV.

Table IV Process and equipment controls in wafer fab

Process step or equipment	Measured attribute	MFG. Inspection	Process control(QC) inspection
Facilities	– Particle counts	—	YES
	– Temperature	—	YES
	– Humidity	—	YES
	– DI Water	—	YES
	– Machine pm's	YES	YES
	– Equipment calibration	YES	YES
Photo	– Critical dimensions(CDs)	YES	YES
	– Alignment	YES	—
	– Resist thickness	—	YES
	– Particles	YES	—
	– Visual Insp	YES	YES
	– Develop check	YES	—
	– Mask visual and defect inspection	YES	YES
Etch	– Power levels	YES	—
	– Temperature	YES	—
	– Gas flows	YES	—
	– Etch rates	YES	—
	– Selectivity	YES	—
	– Etch Insp	YES	—
	– Final Insp	YES	YES
	– Defects	YES	YES
Oxidation	– Temperature	YES	—
	– Temperature profile	—	—
	– Gas flows	YES	—
	– C/V monitors	YES	—
	– V/I monitors	YES	—
	– Film thickness	YES	YES
	– Visuals	YES	—
	– Particle	YES	—
Ion implant	– V/I monitors	YES	—
	– C/V monitors	YES	—
	– E-test	YES	—
Metallization	– Thickness	YES	—
	– Reflectivity	YES	—
	– Step coverfage	—	YES
	– Electromigration	—	YES
CVD	– Thickness	YES	YES
	– Wt% of PSG	YES	YES
	– Refractive index	YES	YES
	– Stress	—	YES
Wafer back-side prep.	– Wafer thickness & finish	YES	YES
	– Back side metal resistivity	YES	—
Outgoing	– 100X MFG. Visual	YES	—
	– 100X QC outgoing visual	—	YES

Note: Where inspection is peformed, it is normally done once per each work shift. MFG. represents Manufacturing

3.6.4.4.1 Photo/Etch process control

Figure 5. schematically illustrates the process steps in a typical photo/etch operation. Each step is carefully monitored for proper equipment settings, preventive maintenance, and calibration. The final thickness and integrity of the photoresist layer are measured and inspected by QC. After develop, "Develop Check" inspection verifies proper exposure and critical dimensions (CDs).

PROCESS CONTROL PROGRAM

The subsequent ion implant and/or etch operation is performed and the photoresist removed by wet or plasma etch techniques.

"Final Check" is performed by QC on every lot to verify the final CDs are correct and material removal is complete. Possible un/over etch, residual photoresist and masking defect (mask, expose, or photoresist-related) are also checked.

Fig 5. Control items in photo/etch process.

Process Flow	Process Step	MFG. Control Item	QC Monitor/Gate
○	Prebake	Oven PM, Temperature, Time, N2 Flow Rate	
○	Photoresist – Spin	Machine PM	Thickness, Pinhole
○	Soft Bake	Oven PM, Temperature, Time	
○	Align/Expose	Light Uniformity Alignment, Focus Test, Mask Clean Inspection, Mask Clean Exposure, Light Intensity	
○	Develop	Equipment PM Solution Control	
□	Develop Check	Photoresist Critical Dimensions, Particles, Mask and Resist Defects	
◇	QC Inspection		Critical Dimension
○	Hard Bake	Oven PM, Temperature, Time, N2 Flow Rate	
○	Etch	Equipment, PM & Settings, Etch Time To Clean	Etch Rate
□	Over/Under		
○	Photoresist	Machine–PM	
□	Final Check	CD's, Over and Under Etch, Particles, Photoresist Residue, Defects, Scratches	
◇	QC Inspection		Same as Final Check. However, more Intense on Limited Sample Basis (AQL 4.0%)

Note: PM represents preventive maintenance

3.6.4.4.2 Gate oxidation process control

Gate oxide integrity is obviously of prime concern to the reliability of MOS device. The preclean step consisting of an acid dip followed by a series of rinses is carefully monitored for acid strength, DI water cleanliness and spin-rinse dryer operation.
Particle counts are taken at all steps of the oxidation process.
Furnace preventive maintenance is performed per a rigid schedule.
This includes temperature profiles and C/V monitors sensitive to contamination.
Fig6. illustrates the process flow at this step.
Final gate oxide thickness are measured on every run, and trended on statistical control charts with warning and actual process shut down limits.
Final gate oxide thickness measurement equipment is calibrated and checked routinely. Further down stream in the process, after metallization is in place, there are specific electrical tests performed on test structures to evaluate oxide properties and defect densities.
Oxide integrity is also evaluated at Wafer Sort where special electical stressing, designed to cause fallout on falut product, is performed.

	MFG. & QC checks
preclean	etch rate, equipment PM, D.I water purity, particle counts
oxidation	furnace PM, temperature profile, C/V monitors, furnace setting, push-pull rates, water loading
thickness measure	thickness measurement, particle counts, measuring equipment calibration

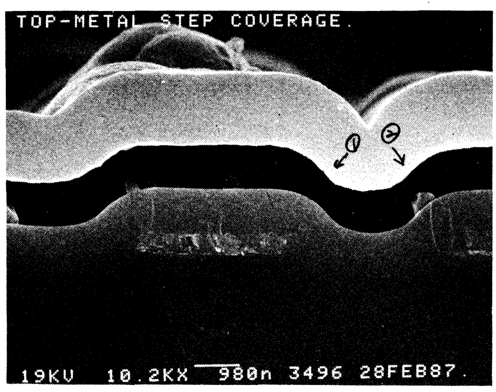
Fig. 6. Gate oxidation process flow.

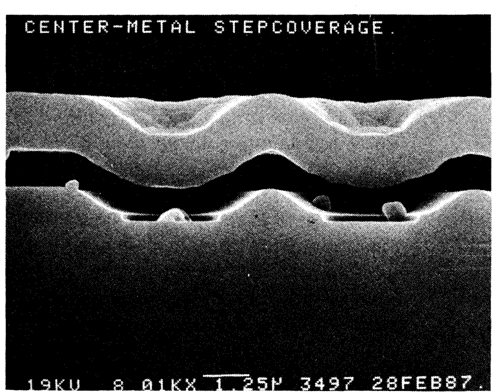
3.6.4.4.3 Reliability-related interlayer Dielectric, Metallization, and Passivation process control.

Issues specific to reliability which are carefully monitored in cooperation with the wafer Fab Reliability group are:

Weight percent phosphorus content of the dielectric glass
Metallization integrity/defect density
Al step coverage
Passivation thickness and step coverage
Film stress
Passivation pin hole
Residual resistance in the metallization process
Electromigration

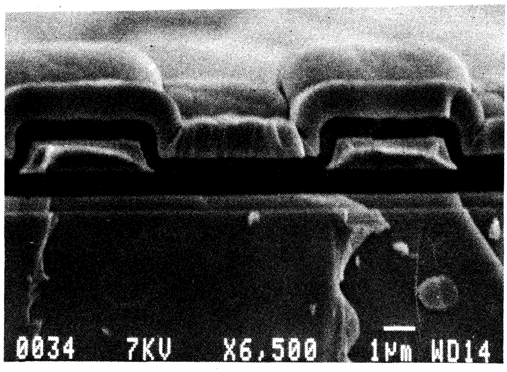
The Fab QC publishes Q&R monitor reports for Fab critical parameters on a weekly or monthly basis. A phosphosilicate glass wt.% P control chart is drawn on line. Following picture show a typical Al step coverage measurement performed by Fab. QC.





Al step coverage monitor performed by QC/QA

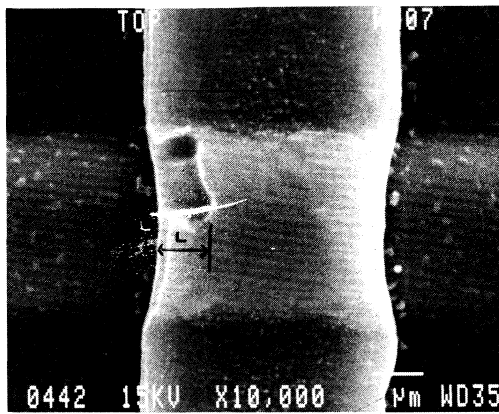
Both passivation thickness and metal etching profile for passivation step coverage are monitored on a weekly basis by Fab. QC.
Following picture show the passivation thickness and metal etching profile.



(a) Metal wet etching

(b) Metal Dry etching and Ashing.

Following picture shows Metal surface/top side view.
The Reduction of an effective metal line cross-sectional area is monitored for the process with Nitride passivation layers. Both reduction of an effective metal line cross-sectional area and difect density data are regularly trended.

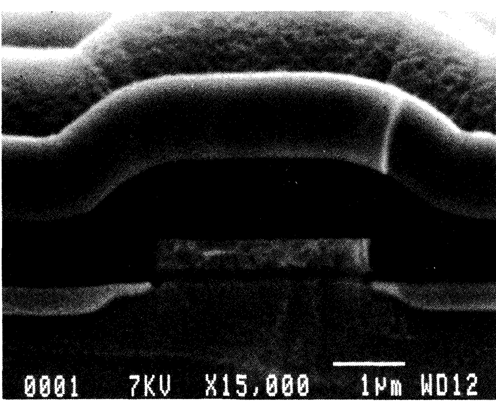


The Reduction of an effective metal line cross-sectional avea.

Passivation pin hole, Film stress, Electronigration, and Residual Resistance (in the metallization process) data are simillarly trended.

MOS process cross section/Junction profile.

SEM micrographs of transfer cross-sections in the following picture illustrate the effective channel length and the LDD (Lightly doped drain) which has occurred in qualifying of HMOS products.



3.6.4.4.4 Process audit (check)

1) Equipment checks

The manufacturing & QC sections have the responsibility for regular equipment checks which verify that operations are being run within specified settings and parameters.
The Q.C section also assures that necessary preventive maintenance procedures have been performed on schedule, and that the equipment is in calibration.

2) Proces control item check

Important process control items must be specified on control charts prepared by the manufacturing section. QC audits these control charts regularly and verifies corrective actions for out of spec. and/or control limit issues.

3.6.4.4.5 Manufacturing equipment qualification

Q.C has the responsibility for manufacturing equipment qualification. This applies to not only manufacturing equipment for wafer production, but also new manufacturing equipment.

Fig. 6. General wafer fabrication flow

Process Flow	Process Step	Major Control Item
	Wafer and Mask Input	
	Starting Material Incoming Inspection	Wafer(See 3.6.1) Mask (See 3.6.2)
	Wafer Sorting and Labeling	Resistivity
	Initial Oxidation	Oxide Thickness
	Photo	See 3.6.4.4.1
	Inspection	Critical Dimension Visual/Mech AQL 4.0%
	QC Gate	Critical Dimension
	Etch	See 3.6.4.4.1
	Inspection	Critical Dimension Visual/Mech AQL 4.0%
	QC Gate	Critical Dimension Visual/Mech
	Diffusion Metallization	See Table IV
	E-Test	Electrical Characteristics

Fig. 6. General wafer fabrication flow (continued)

Process Flow	Process Step	Major Control Item
	Back–Lap	• Thickness
	Back Side Evaporation	• Thickness, Time, Resistivity Evaporation Rate
	Final Inspection	• All Wafers Screened (Visual/Mech)
	QC Fab Final Gate	• Visual/Mech. AQL 4.0%
	EDS (Electrical Die Sorting)	
	QC Monitor	• Function Monitor • Ink Dot Size • Height of Probe Tip • Operability of Probe Tip • Misalignment
	Sawing	
	QC Monitor	• Sawing Depth • D.I. Water Purity • Bacterial Count • CO_2 Bubbler Purity • Visual
	Inspection	Die Screen
	QC 2′ nd Optical	• AQL 1.0% Fab Defect Test Defect Sawing Defect

3.6.4.5 Shipping procedure for uncapsulated chips

3.6.4.5.1 Packing option

There are three kind of packing forms.

Waffle pack

This is a 2X2 waffle type carrier with a seperate hole for each die.
Chips are 100% visually inspected with the rejects removed.

Wafer pack

The pack contains a wafer that is 100% electrically tested.
With the rejects inked, the wafers is left unsawed and packaged with protective cardboard in a vacuum sealed plastic bag.

Jar pack

The pack contains 25 wafers(Max.) that are 100% electrically tested.
With the rejects inked, wafers are left unsawed and packaged with protective Jar.
Each wafers are seperated by filter paper.

3.6.4.5.2 Visual Inspection

All dies go through extensive visual inspection during die processing. (See flow chart)
Dies are inspected at 50X to 100X magnification using SAMSUNG's standard visual inspection criteria which is based on MIL-STD 883C.
Copies of the visual inspection documents are available upon request.

Visual Lot Inspection Gates

Step	Basic Magnification	Production Inspection Volume	QC Inspection Gate
Fab inprocess	200 X	All wafers	All lots
Fab outgoing	100 X	All wafers	All lots
Die visual after sawing (2'nd optical)	50~100 X	All chips(100%)	All lots

Line operators also peform a variety of visual inspection monitors of the quality of their Fab and sawing process and product.
The disposition of material failing visual lot inspection gates is 100 percent rescreening (Wafer/Chip).
Visual Inspection monitor issues are tracked by an ITR (Inspection Trouble Report) system, which prescribes suitable corrective actions.
Defect levels in each visual gate are tracked and reported on a weekly or monthly basis causes of specific defects are identified and resolved.

3.6.4.5.3 Storage and handling precautions

It is recommended that all SAMSUNG die be stored at room temperature in an inert environment after removal of the seal from the original shipping package. Special Electro-static Discharge(ESD) precautions should be taken to avoid damage the chips.
SAMSUNG recommends storage in the original ESD shipping package.
Extreme care must be required in handling unencapsulated semiconductors to avoid damage to the chip surface.
The following precautions apply.

Waffle pack

Lid and anti-static mylar should be removed slowly and extreme care to avoid disturbing position of the die.
Dies should be handled with smooth tipped vacuum wand only.
Do not use tweezers.

Wafer pack/Jar pack

Wafer should only be handled near edge with round-ended stainless steel or teflon tweezers.
SAMSUNG recommend to use the finger-cot.

VISUAL INSPECTION FLOW CHART

Wafer inventory

Preselection visual and electrical 100% wafer

100% probed and inked

Ink curing

Visual inspection

Electrical QC acceptance

Wafer Pack	Jar Pack	Waffle Pack
Prepacking wafer	Prepacking wafer	Wafer sawing
Visual QC acceptance	Visual QC acceptance	Waffle pack loading
Wafer packing	Jar packing	Prepacking dice
QC acceptance	QC Acceptance	Final Q.C. visual (100% acceptance)
Store	Store	Store

Fig.	Jar label Jar filter paper	label Lint free paper PAD	mylar paper chip Carrier
option	Jar pack	Wafer pack	Waffle pack
Method	each lot (25 wafers, max.)	each wafer	carrier with a seperate hole for each die.
products	• MOS • L-IC	• MOS • L-IC • TR	• MOS • TR (Die size is larger than 4000μx4000μ)
Document	EDS summary is in a Jar.	EDS summary is in a box.	—
Remark	Packed with vinyl.	Packed with antistatic box.	Antistatic case (transparent)

Packing Method Comparison

3

3.7 Process Control—Assembly

3.7.1 Process control and inspection points of the assembly operation are explained and listed below.

1) Die inspection
   Following 100% inspection by manufacturing, in-process quality control samples each lot according to internal or customer specifications and standards.
2) Die attach inspection
   Visual inspection of samples is done periodically on a machine/operator basis. Die attach techniques are monitored and temperatures are verified.
3) Die shear strength
   Following die attach, die shear strength testing is performed periodically on a machine/operator basis. Either manual or automatic die shear stressing is used.
4) Wire bond inspection
   Visual inspection of samples is complemented by a wire pull test performed periodically during each shift. These checks are also done on a Machine/Operator Basis, and $\bar{X}R$ data is derived.
5) Pre-Seal/Pre-Encapsulation inspection
   Following 100% inspection of each lot, samples are taken on a lot acceptance basis and are inspected according to internal or customer criteria.
6) Seal inspection
   Periodic monitoring of the sealing operation checks critical temperature profiles of the sealing oven for both glass and metal seals.
7) Post-seal inspection
   Subsequent to a 100% visual inspection, in-process quality control samples each lot for conformance to visual criteria
8) General assembly flow is shown in Fig. 7.

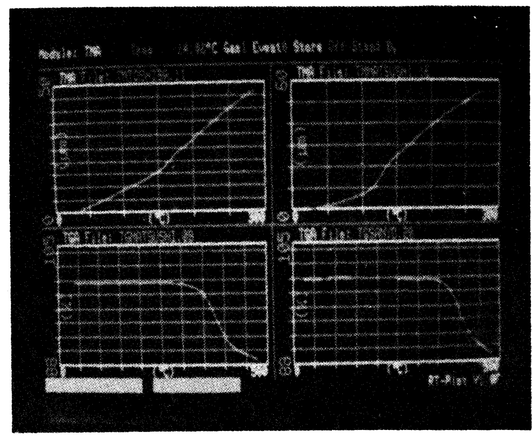
3.7.2 Sampling plans

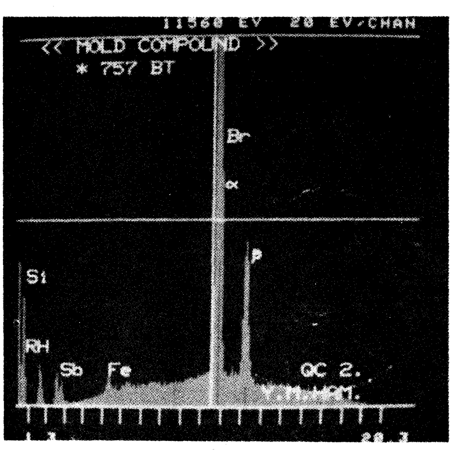
1) Sampling plans are based on an AQL(acceptable quality level) concept, and are determined by internal or customer specifications.
2) Raw material incoming inspection
   See Table V.

Table V Raw material inspections

Material	Inspection Item	Acceptable Quality Level
Lead Frame	1) Visual Inspection 2) Dimension Inspection 3) Function Test 4) Work Test	LTPD 10%,C=2 LTPD 20%, C=0 LTPD 20%, C=0 LTPD 20%, C=0
Wafer	1) Visual Inspection	AQL 0.65 %
Au/Al (Wire)	1) Visual Inspection 2) Bond Pull Strength Test 3) Bondability Test 4) Chemical Composition Analysis	LTPD 20%, C=0 LTPD 15%, C=2 LTPD 1.5%, C=6 N=4, C=0
Molding Compound	1) Visual Inspection 2) Moldability Test 3) Chemical Composition Analysis	N=5, C=0 Critical Defect: 0.15% Major Defect: 1.0% Minor Defect: 1.5% N=5, C=0
Packing Tube & Pins	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Function Test	N=20, C=1 N=10, C=0 N=10, C=0 N=10, C=0
Solder	1) Visual Inspection 2) Weight Inspection 3) Chemical Composition Analysis	AQL 1.0 LTPD 20%, C=0 LTPD 20%, C=0
Flux	1) Acidity Test 2) Specific Gravity Test 3) Chemical Composition Analysis	LTPD 20%, C=0 LTPD 20%, C=0 LTPD 20%, C=0
Solder Preform	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 2.5% AQL 2.5% AQL 2.5%
Coating Resin	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 0.65% AQL 0.65% AQL 0.65%
Marking Ink	1) Work Test Major Defect: 1.0% Minor Defect: 1.5% 2) Mark Permanency Test	Critical Defect: 0.15% N=5, C=0
Chip Carrier	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test 5) Work Test	AQL 2.5 AQL 0.65 N=10, C=0 N=5, C=0 AQL 0.65
Vinyl Pack	1) Visual Inspection 2) Work Test 3) Electo-Static Inspection	LTPD 20%, C=0 LTPD 20%, C=0 LTPD 15%, C=0
Ag Epoxy	1) Work Test 2) Chemical Composition Analysis	N=8, C=0 N=8, C=0
Letter Marking	1) Visual Inspection 2) Work Test	All Inspection
Spare Parts & Others	1) Dimension Inspection 2) Visual Inspection	N=5, C=0 N=5, C=0

3





Molding Compound Incoming Inspection Results
TA(DUPONT 9900), EDXRF(LINK XR-500)

3) In-Process Quality Inspection

A. Assembly lot acceptance inspection

(1) Acceptance quality lével for wire bond gate inspection

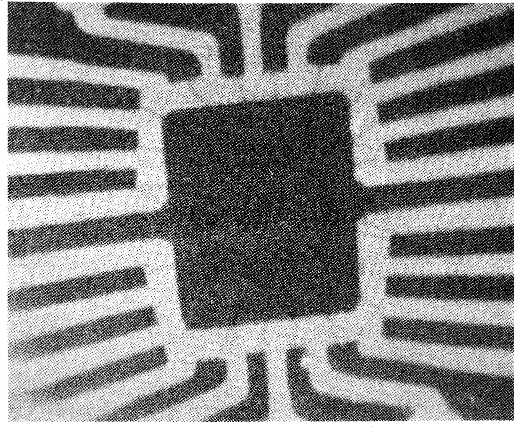
Defect Class	Inspection Level	Defect Items	
Critical Defect	AQL 0.65%	– Missing Metal – Chip Crack – No Probe – Epoxy on Die – Mixed Device – Wrong Bond – Missing Bond	– Diffusion Deffect – Ink Die – Exposed Contact – Bond Short – Die Lift – Broken Wire
Major Defect	AQL 1.0%	– Metal Missing – Metal Adhesion – Pad Metal(Discolored) – Tilted Die – Die Orientation – Partial Bond	– Oxide Defect – Probe Damage – Metal Corrosion – Incomplete Wet – Weakened Wire
Minor Defect	AQL 1.5%	– Adjacent Die – Passivation Glass – Die Attach Defect – Wire Loop Height – Extra Wire	– Contamination – Ball Size – Wire Clearance – Bond Deformation

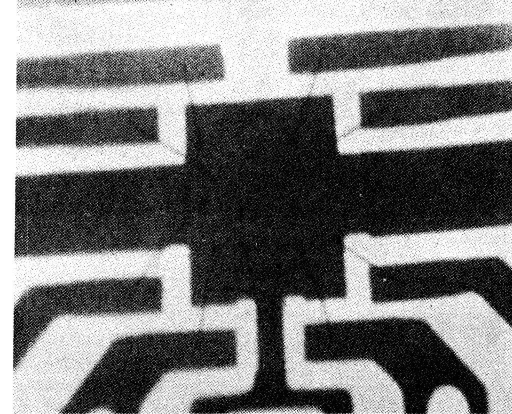
(2) Acceptance quality level for mold/trim gate inspection

Defect Class	Inspection Level	Defect Items
Critical Defect	AQL 0.04%	– Incomplete Mold – Deformation – Void, Broken Package – No Plating – Misalignment – Broken lead
Major Defect	AQL 0.25%	– Ejector Pin Defect – Crack, Lead Burr – Package Burr – Rough Surface – Flash on Lead – Squashed Lead
Minor Defect	AQL 0.40%	– Lead Contamination – Bent Lead – Poor Plating – Package Contamination

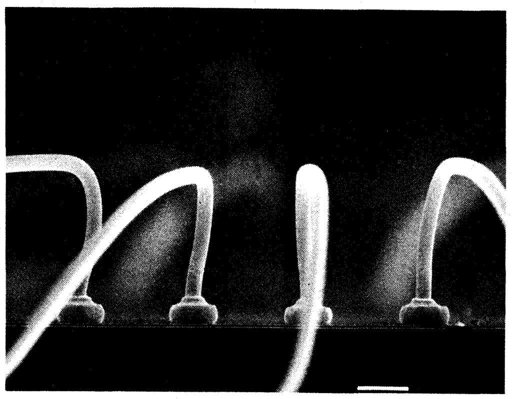
B. In-process monitor inspection

Inspection Item	Frequency	Reference
• Die Shear Test	Each Lot	MIL-STD-883C, 2019
• Bond Strength Test	1 Time/Shift/Each Equip	MIL-STD-883C, 2011
• Solderability Test	Weekly	MIL-STD-883C, 2003
• Mark Permanency Test	Weekly	MIL-STD-883C, 2015
• Lead Integrity Test	Weekly	MIL-STD-883C, 2004
• In-Process Monitor Inspection for Product	1 Time/Shift/Each Process	Verify Relative to Control Unit
• X-Ray Monitor Inspection for Molding	1 Time/Shift/Mold Press	Verify Relative to Control Unit
• Monitor Inspection for Production Equipment	2 Times/Shift/Each Unit of Equipment	Verify Relative to Control Unit

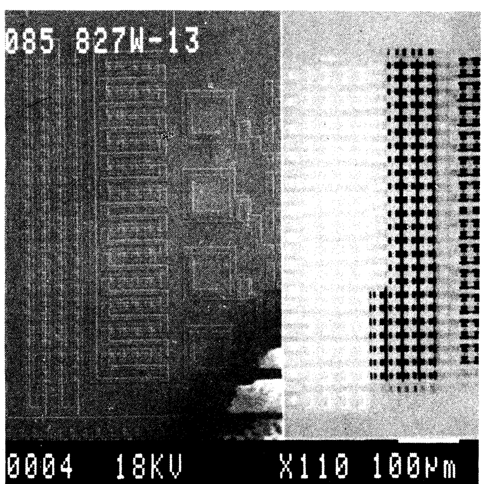




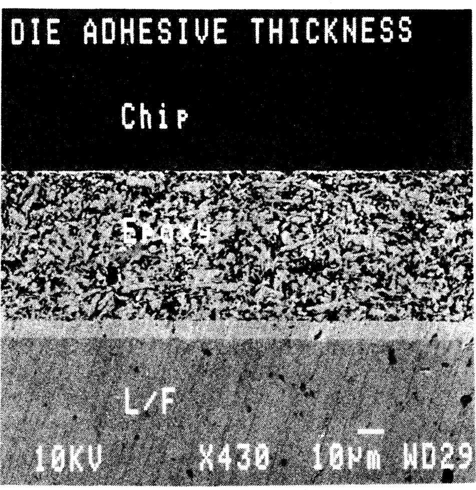
X-Ray Monitor Results
(Model: MG161, PHILIPS)



WIRE BONDING MONITOR BY SEM
(MODEL JSM IC-845, JEOL)



APPLICATION OF SEM



DIE ADHESIVE THICKNESS MONITOR

4) Outgoing quality inspection plan(LTPD)

Defect Class		Discrete	LSI	Kind of Defect
Critical	Electrical Visual	1%	2%	Open, Short, Wrong Configuration No Marking
Major	Electrical Visual	1.5%	3%	Items which affect reliability most strongly
Minor	Elec Visual	2%	5%	Items which minimally or do not affect reliability at all (Cosmetic, Appearance, Etc...)

Fig. 7. General assembly flow

Process Flow	Process Step	Major Control Item
	Wafer	
	Wafer Incoming Inspection	Q.C Wafer Incoming Inspection, AQL 4.0%
	Tape Mount	
	Sawing Q.C. Monitor	Q.C Monitoring – Chip-Out – Scratch – Crack – Sawing Discoloration – Sawing Speed – Cut Count – D.I. Water purity – CO_2 Bubble Purity
	Visual Inspection	100% Screen: – FAB Defect – EDS Test Defect – Sawing & Scratch Defect
	Q.C. Gate	1st AQL: 1.0% Reinspection AQL : 0.65%
	Leadframe	
	Leadframe Incoming Inspection	Q.C. Lead Frame Incoming Inspection • Acceptance Quality Level – Dimension : LTPD 20%, C=0 – Visual & Mechanical : LTPD 10%, C=2 – Functional Work Test : LTPD 10%, C=2
	Die Attach	
	Q.C. Monitor	Q.C. D/A Monitor Inspection • Bond Force • Frequency 1 Time / Station / Shift • Sample : 24 ea/time • Acceptance Criteria

Defect	Acceptance	Reject
Critical	0	1
Major	1	2

Fig. 7. General assembly flow (Continued)

Process Flow	Process Step	Major Control Item
	Cure	
	Q.C. Monitor	Q.C. Cure Monitor Inspection 1. Control Item – Temperature – In/Out Time 2. Frequency – 1 Time/Shift
	Au Wire	
	Bonding Wire Incoming Inspection	Q.C. Wire Incoming Inspection 1. Visual Inspection : LTPD 20%, C=0 2. Bond Pull Strength Test: N=15, C=2 3. Bondability Test LTPD 1.5%, C=6
	Wire Bonding	
	100% Visual Inspection	
	Q.C. Monitor	Q.C. Wire bond Monitor Inspection Frequency : 3 Times/Machine/Shift
	Q.C. Gate	Q.C. Acceptance Quality Level – Critical Defect : AQL 0.65% – Major Defect : AQL 1.0 % – Minor Defect : AQL 1.5 %
	Mold Compound	
	Incoming Inspection	Moldability Test – Critical Defect : AQL 0.15% – Major Defect : AQL 1.0 % – Minor Defect : AQL 1.5 %
	Mold	
	Q.C. Monitor	Q.C. Mold Monitor Inspection 1. In-Process Monitor Inspection – Frequency : 3 Times/Station/Shift – Sample : 1 Shot/Time 2. Acceptance Quality Level – Critical Defect : AQL 0.065% – Major Defect : AQL 0.25%
	Cure	
	Q.C. Monitor	Q.C. Cure Monitor Inspection 1. Control Item – Temperature – In/Out Time 2. Frequency – 1 Time/Shift
	Deflash	

Fig. 7. General assembly flow (Continued)

Process Flow	Process Step	Major Control Item
	Q.C. Monitor	Q.C. Deflash Monitor Inspection 1. Control Item – Pressure – Belt Speed – Visual/Mechanical Inspection 2. Frequency : 3 Times/ Machine/Shift 3. Identify Each Defect Control Limit
	Trim/Bend	
	Q.C. Monitor	Q.C. Trim/Bend Monitor Inspection 1. Visual Inspection. 2. Frequency : 3 Times/Station/Shift
	Solder	100% Visual Inspection
	Q.C. Monitor	Q.C. Solder Monitor Inspection 1. Frequency : 3 Times/Station/Shift 2. Criteria – Critical Defect : AQL 0.65% – Major Defect : AQL 1.0 %
	Q.C. Gate	Q.C. Mold Gate – Acceptance Criteria Critical Defect : AQL 0.04% Major Defect : AQL 0.25% Minor Defect : AQL 0.40%
	Test	100% Electrical Test
	Q.C. Monitor	Correlation Sample Read Prior to Initial Device Test
	Mark	100% Visual Inspection
	PRT Monitoring (Process Reliability Testing)	1. PRT for LSI – HOPL (168 HR) – PCT (48 HR) – Other (When Applicable) 2. Acceptance Criteria : LTPD 10%
	Q.C. Monitor	Q.C. Marking Monitor Inspection – Frequency : 3 Times/Station/Shift – Sample : 50 Units/Time – Acceptance Criteria <table><tr><th>Defect</th><th>Acceptance</th><th>Reject</th></tr><tr><td>CRITICAL/ MAJOR</td><td>0</td><td>1</td></tr></table>
	Q.C. Gate	Q.C. Final Acceptance Level – Critical Defect : AQL 0.065% – Major Defect : AQL 0.40% – Minor Defect : AQL 0.65%

Fig 7 General assembly flow (continued)

Process Flow	Process Step	Major Control Item
	Q.A. Gate	Q.A. Incoming Inspection for LSI 1. Critical Defect – Electrical Test : LTPD 2% (N=116, C=0) – Visual Test : LTPD 2% (N=116, C=0) 2. Major Defect – Electrical Test : LTPD 3% (N=116, C=0) – Visual Test : LTPD 3% (N=116, C=0) 3. Minor Defect – Electrical Test : LTPD 5% (N=116, C=2) – Visual Test : LTPD 5% (N=116, C=2)
	Stock	Age Control
	Q.A. Gate	Q.A. Outgoing Inspection 1. Quality 2. Customer 3. Packing 4. Sampling Inspection (When Applicable) – Sampling Plan is Same as Incoming Inspection
	Shipment	

3.8 Material Control

3.8.1 General

It is the policy of Samsung to assure conformance of materials to technical requirements. The extent and type of assurance inspection is based upon evidence of the supplier's degree of quality control, as well as the criticality of the material.

3.8.2 Policies

Samsung quality control is responsible for five key areas of incoming material quality. They are detailed below.

1) Establishing procedures to address material identification and integrity.
   - A. Provide adequate inspection and testing methods.
   - B. Assure segregation within production operation regarding materials undergoing inspection, uninspected materials, and non-conforming materials.
   - C. Provide for identification of approved materials until processing or fabrication obliterates identity. The purity grade-electronic grade is used unless another grade is specified in the process specification.

2) Incoming inspection

   All materials and pieceparts purchased for production, with the exception of chemicals and gases, must pass through incoming inspection. There they are tested according to the appropriate purchase or incoming inspection specification. As it is not possible to determine the quality of certain items by normal inspection techniques, sometimes additional manufacturing tests are undertaken, which are monitored by quality control. Batch control is maintained when necessary, and the quality is monitored where possible via in-line checks of production processes. The quality department retains the right to carry out acceptance tests on chemicals, but its policy is not to analyze incoming chemical materials as a general practice.

3) Rejection/Waiver

   When a batch of materials or piece parts fails to meet the incoming inspection specification, it is the responsiblity of the incoming inspection group to inform production control, engineering, purchasing and the QC manager of the failure. This is done via distributed documentation. The detailed report provides data for QC and process engineering to assess the criticality of the fault, and its probable effects on quality, yield and cost. If a waiver to accept nonconforming material is considered, a request is initiated by production control, who must obtain the approval of the process engineer, quality control engineer and operating superintendant. In the event of any disagreement at this level, final disposition is by consensus of the quality and manufacturing managers.

4) Non-conforming items

   All incoming material is held in quarantine in the incoming inspection section until it is accepted and placed in storage, or rejected and sent out of the factory. Only approved and accepted piece parts and materials are allowed to reach the warehouse.

5) Issue from warehouse

   Every consignment in the warehouse bears an incoming lot number, which can be used to refer to an incoming inspection report. Issuance of all batches is in chronological order.

3.9 Vendor Relations

It is company policy to encourage cooperation between suppliers and Samsung to achieve high quality at low cost. This is implemented via the methods discussed below.

3.9.1 All purchases of production material and pieceparts are made to formal specifications. These specifications specify requirements and give the supplier full details of incoming inspections and AQL's.
3.9.2 When a new supplier is approached where critical pieceparts are concerned, or a new requirement arises, the specification is discussed with the supplier to ensure that the specification is understood and attainable.
3.9.3 All incoming batches of production material are examined on receipt, and the results of incoming inspections are reported back to the supplier. This is done in the event of batch rejection, observed but non-rejectable faults, and in other cases where feedback of information is considered as necessary.
3.9.4 Visits are made to supplier premises whenever it is deemed appropriate to ensure quality.
3.9.5 It is company policy to encourage suppliers to institute quality improvements and cost reductions in cooperation with Samsung.

3.10 Control of Finished Product

3.10.1 The company approach to the control of finished devices is that the production department make and completely test all devices. Product is then directed in batches to the quality final acceptance group, who decide on the basis of a predetermined sample plan whether the product is fit for sale. Although a waiver can be issued at this late stage in the case of standard commercial product, it is Samsung's policy that such waivers are given only under very exceptional circumstances. Full details of any such waiver are recorded, and the waiver itself can only be given with the approval of both the quality manager and the marketing manager.

3.10.2 Finished goods procedure

1) Devices are delivered from the assembly area to the test shop in assembly batches split from a fabrication batch. In the case of low volume devices, several fabrication batches may be combined to produce an assembly batch of economical size. Subsequent to assembly, devices are electrically tested, marked, and bagged or reeled. A separate acceptance procedure is carried out before release into storage as described in 3.7.2
2) Devices for release into storage are made up into a release batch in quantities determined by production control. These release batches are packed on reels (taping transistor), in plastic bags (transistors and ICs), and in transport tubes(ICs) within labelled cartons. Product is then delivered to a designated place in the final acceptance area together with a partially filled-out lot traveller card. Final acceptance personnel carry out electrical and visual sampling. It is checked and established that device codes on the devices correspond with those on the documentation, and that the quantity of devices corresponds to the figures on the lot traveller card. If the batch is accepted, package labels and the lot traveller card are stamped, and the batch with its documentation is approved for released product, from whence it is transported to the finished goods warehouse.
   Rejected batches are returned for test with documentation demonstrating the cause for rejection. Here parts are 100% retested, and quantities corrected on the accompanying documentation. Devices are then resubmitted together with the original rejection ticket. Devices elimated during retest are scrapped. Both for accepted and rejected batches the results of testing are entered daily into a computer databank, and are analyzed to produce daily, weekly and monthly historical quality statistics.

3) Standard commercial product sampling is carried out in accordance with MIL-STD 19500E. Applicable LTPD and inspection levels for the various product classes are specified in documentation issued by the quality department.
4) The acceptance test supervisor is issued a copy of all internal electrical test specifications. No product is accepted unless an electrical specification exists.
5) Product is normally tested on electronically-or computer-controlled equipment, with the test program taking the form of a program on a program board, paper, or magnetic tape. Test documentation in each case contains the appropriate type of identification together with a reference to the internal electrical test specification and revision.

3.11 Inspection Control

3.11. Training of inspectors

An inspector's supervisor is required to explain the objectives and significance of each particular inspection specification in relation to the performance of the product and the manufacturing process. Additionally, he/she must explain and demonstrate the requirements of the specification, using appropriate samples and aids. Details covered include sampling procedures, inspection levels, visual quality standards, mechanical, electrical and other tests, set-up, calibration and use of equipment, disposition of inspection work, and corrective action procedures as required. The supervisor must be satisfied that the inspector is competent to perform the inspection according to the appropriate specification before allowing him/her to operate.

3.11.2 Evaluation of inspectors

The work of production inspectors is subject to frequent audits by quality control inspectors. Performance is monitored such that corrective action can be taken if required.

Monitoring is done informally on a day-to-day basis. It's also done more formally for other intervals by the supervisor via means appropriate to the particular inspection or test.

3.12 Calibration

3.12.1 General purpose

To provide a system whereby production and test equipment parameters are correlated to Samsung standards via internal and external calibration methods.

3.12.2 Responsibility of calibration

1) Calibration of manufacturing and test equipment is the superintendent's responsibility of the respective process engineering and test engineering departments. It is carried out by either test engineering or an extrnal service organization.
2) Calibration of equipment used for quality control for piece parts, incoming raw material, in-process quality measurement, final acceptance, and batch release of product is the responsibility of the quality department. It is carried out by either QC or external organizations.

3.12.3 Calibration system of the quality department.

1) All equipment registered is classified into one of the following categories.

Class A – Equipment used as a measurement tool or physical standard. Instrumentation used for the calibration of class B equipment (e.g., differential voltmeter standard cells). These standards are calibrated regularly against national standards, which in turn are traceable to international standards.

Class B – Equipment associated with calibration of class C equipment (e.g., resistance boxes, voltmeters)

Class C – Equipment directly associated with product specification testing (e.g., QC test gauge)

2) A centralized set of records for all registered equipment is held by QC.
3) The calibration group of the QC department is responsible for informing the maintenance group of:
   a) The need for maintenance or repair on registered equipment
   b) Movement of registered equipment
   c) Acquisition of new equipment requiring registration
4) Equipment registered carrying labels signifying calibation is performed on a routing basis.
5) Calibration frequency is determined from information contained within calibration records. Frequencies are controlled by quality standards.

3.12.4 Procedure

1) Calibration is conducted by qualified personnel only. Comprehensive specifications for procedural methods are made available for complex instrumentation systems.
2) A Calibration record contains reference to:
   A. Operational and calibration status
   B. Frequency of Calibration
   C. Dates applicable
   D. Personnel involved
3) In addition to an individual calibration record for each piece of registered equipment, a display chart showing the current calibration status of all registered equipment is maintained.

3.12.5 Calibration labels

Label coloring determines instrument grade as shown in Fig. 8.

Color	Grade
White	General Instrument
Yellow	Precision Instrument
Blue	Working Standard

Calibration	Certificate
Control No.	
Model No.	
Serial No.	
Data of Cal.	
Recal. Date	
	Standard Instrument Laboratory by SST

Fig. 8. Calibration Labels

CHAPTER IV QUALITY ASSURANCE and RELIABILITY PROGRAM

4.1 Introduction

Samsung utilizes rigorous qualification and reliability programs to monitor the integrity of its devices. All industry standard (and various non-standard) stresses are run. Testing is done not only to collect data, but also to detect trends and product anomalies, with rectification to take place immediately (if necessary). This protects the customer from receiving discrepant material. Careful attention is given to any manufacturing changes, both through Engineering Change Notices and appropriate reliability stressing.
Items such as particular tests, frequency, sample sizes, acceptance criteria, and methods of stressing are detailed later in this chapter.

4.2 Policy

Samsung is committed to supplying high-quality semiconductors to its consumers. All product released for general sales has been fully tested and qualified. By meeting or exceeding normal industry standards for reliability, Samsung can confidently supply products to the world that will meet customer applications and reliability standards. Of course special programs can be run for customers who have particular requirements which are considered non-standard.
The quality organization must approve any product before it is officially qualified and distributed. To do this most effectively, fully-functional devices must pass two critical stages prior to sales. Step 1 is product evaluation; step 2 is product qualification. Details are listed below.

4.3 Scope

Pass/Fail criteria are established by the quality assurance organization. All products have specifications which apply to then regarding reliability stressing, periodical monitoring, and final lot disposition.
The quality department is responsible for investigating mass-produced product for discrepancies, and enforcing corrective actions. All outgoing product goes through "QA-gating", where tests particularly critical to the product are accomplished. Only when quality assurance approves a device, either through qualification or gating acceptance, is it released. Fundamental "no-rework" policies ensure only highly reliable material leaves the factory. Testing is done to MIL-STD 883 and MIL-STD 750 standards, with sampling done in accordance with MIL-STD 19500E and MIL-STD 105D. Samsung also has internal specifications where its requirements exceed those of MIL-STDs.

4.4 Qualification Procedures

Procedures to qualify devices are listed below. There are both general and product-specific requirements. Procedures are detailed for new products, die-only qualifications, and package-only qualifications. The latter two are for products and/or packages already qualified, but where there is room for further product optimization.

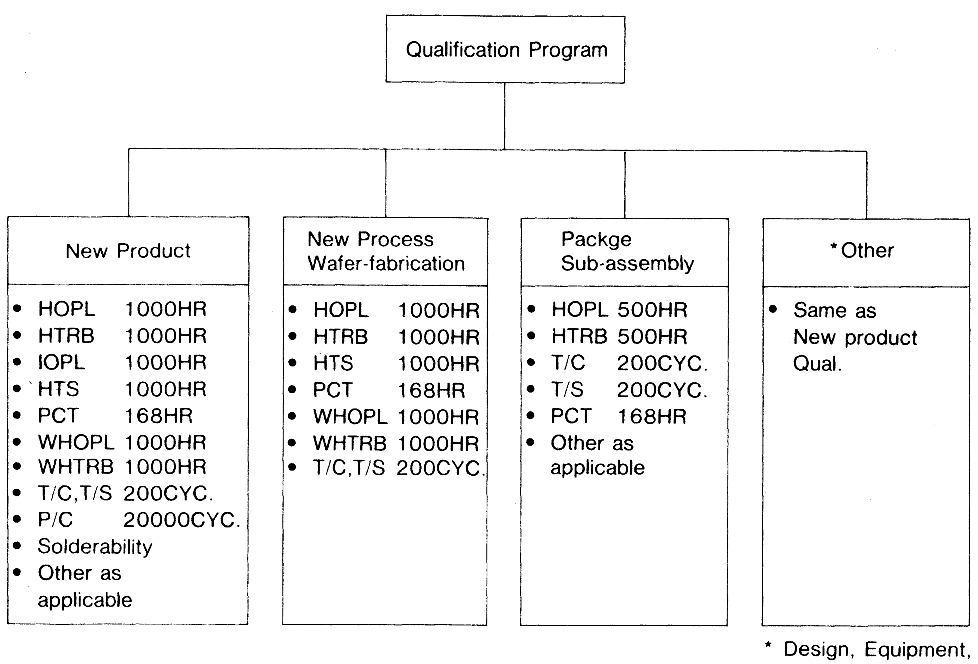


Fig 9. Qualification Programs.

QUALITY ASSURANCE and RELIABILITY PROGRAM

A) New product qualification test items

No.	Test Item	Test Condition	Part		Sample Size	LTPD	ACC. No	Reference Method	Note
			L-IC	Discrete					
1	High Temperature Reverse Bias (HTRB)	$Ta=T_j(max)$ $V_{CB}=0.8\times V_{CBO}$ 1000HRS	—	YES	45	10	1		48HR for PRT
2	High Temperature Operating Life (HOPL)	$Ta=T_{opr}(max)$ $V_{CC}=V_{CC}(max)$ Static, Dynamic 1000HRS	YES	—	45	10	1	MIL-STD-883 1005	48HR for PRT
3	High Temperature Storage (HTS)	$Ta=T_j(max)$ 1000HRS	YES	YES	45	10	1		
4	Operating Life (OPL)	Ta=25°C Pc=Pc(max) 1000HRS	—	YES	45	10	1	MIL-STD-750 1026.3	For Small-Signal Device
5	Intermittent OPL (IOPL)	Ta=25°C Pc=Pc(max) 2min/2min On/Off 1000HRS	—	YES	45	10	1	MIL-STD-750 1036.3	
6	Power Cycle (P/C)	$\Delta T_j=125°C$ 120Sec/120Sec On/Off 10000CYC.	YES	YES	45	10	1		For PWR TR, PWR IC
7	Pressure Cooker Test (PCT)	Ta=121°C±2°C RH=100% 15PSIG 168HRS	YES	YES	45	10	1		48HR for PRT
8	Wet High Temperature Reverse Bias (WHTRB)	Ta=85°C, RH=85% $V_{CB}=0.8\times V_{CBO}$ 1000HRS	—	YES	45	10	1		
9	Wet High Temperature Operating Life (WHOPL)	Ta=85°C, RH=85% $V_{CC}=V_{CC}(opr)$, Pdmin 1000HRS	YES	—	45	10	1		
10	Thermal Shock (T/S)	−65°C↔150°C (Liquid) 5min,<10Sec, 5min 200 Cycles	YES	YES	45	10	1	MIL-STD-883 1011	
11	Temperature Cycle (T/C)	−65°C↔25°C↔150°C 10min, 5min, 10min 200 Cycles	YES	YES	45	10	1	MIL-STD-883 1011	
12	Solder Heat Resistance (S/H)	Ta=260°C±5°C t=10+2Sec	YES	YES	10	N/A	0	MIL-STD-750 2031.1	
13	Solderability	Ta=245°C±5°C t=5±0.5sec Reject is>10% uncovered surface	YES	YES	10	N/A	0	MIL-STD-883 2003	
14	Salt Atmosphere	Ta=35°C, 5% NaCl 24HRS	YES	YES	10	N/A	0	MIL-STD-883 1009A	

New products qualification test item (Continued)

No.	Test Item	Test Condition	Part		Sample Size	LTPD	ACC. No	Reference Method	Note
			L-IC	Discrete					
15	Mechanical Shock	1500G, 0.5ms 3 Times Each direction of X,Y and Z Axis	YES	YES	10	N/A	0	MIL-STD-750 2016	For Hermetic
16	Vibration	20G, 3Axis f=20 to 2000 cps for 4min, 4 cycles	YES	YES	10	N/A	0	MIL-STD-883 2007	For Hermetic
17	Constant Acceleration	2000G X,Y,Z Axis 1min for each Axis	YES	YES	10	N/A	0	MIL-STD-883 2001	For Hermetic
18	ESD (Human Body Model)	R=1.5kΩ C=100pF 5 Discharge V≥±1000V	YES	YES	5	N/A	0	MIL-STD-883 3015	
19	Latch-up Test		YES	—	5	N/A	0	—	For CMOS
20	Fine Leak Gross Leak	Helium Fluoro carbon	YES	YES	45	10	1	MIL-STD-883 1014	For Hermetic

Note)
- N/A: Not available
- SOT-23, TO-92S PKG: PCT 48HR
- PRT: process Reliability Test (all outgoing Lots)

B) New process, wafer fabrication qualification

No	Test Item	Test Condition	Package		Sample Size	LTPD	ACC No
			L-IC	Discrete			
1	High Temperature Operating Life (HOPL)	$T_a=T_{opr}(max)$ $V_{CC}=V_{CC}(max)$ STATIC, DYNAMIC 1000HRS	YES	—	45	10	1
2	High Temperature Reverse Bias (HTRB)	$T_a=T_j(max)$ $V_{CB}=0.8\times V_{CBO}$ 1000HRS	—	YES	45	10	1
3	High Temperature Storage (HTS)	$T_a=T_j(max)$ 1000HRS	YES	YES	45	10	1
4	Pressure Cooker Test (PCT)	$T_a=121°C\pm2°C$ RH=100% 15 PSIG 168HRS	YES	YES	45	10	1
5	Wet High Temperature Operating Life (WHOPL)	Ta=85°C, RH=85% $V_{CC}=V_{CC(opr)}$ 1000HRS	YES	—	45	10	1
6	Wet High Temperature Reverse Bias (WHTRB)	$T_a=85°C$, RH=85% $V_{CB}=0.8\times V_{CBO}$ 1000HRS	—	YES	45	10	1
7	Thermal Shock (T/S)	$-65°C\rightleftharpoons150°C$(Liquid) 5min, <10sec, 5min 200 cycles	YES	YES	45	10	1
8	Temperature Cycle (T/C)	$-65°C\rightleftharpoons25°C\rightleftharpoons150°C$ 10min, 5min, 10min 200 Cycles	YES	YES	45	10	1

4

C) Package Sub-Assembly Qualification

No	Test Item	Test Condition	Package		Siample Size	LTPD	ACC No	Notes
			Plastic	Hermetic				
1	High Temperature Reverse Bias (HTRB)	$Ta=T_j(max)$ $V_{CB}=V_{CBO}\times 0.8$ 500HRS	YES	YES	45	10	1	For Discrete
2	High Temperature Operating Life (HOPL)	Ta=Topr(max) $V_{CC}=V_{CC}(max)$ Static, Dynamic 500HRS	YES	YES	45	10	1	For L-IC
3	Temperature Cycle (T/C)	−65°C⇌25°C⇌150°C 10min, 5min, 10min 200 CYCLES	YES	YES	45	10	1	
4	Pressure Cooker Test (PCT)	Ta=121°C±2°C RH=100%, 15PSIG 168HRS	YES	—	45	10	1	
5	Thermal Shock (T/S)	−65°C⇌150°C(Liquid) 5min,<10sec, 5min 200 CYCLES	YES	YES	45	10	1	
6	Solder Heat Resistance (S/H)	260°C±5°C 10±1 sec Once without Flux	YES	YES	10	N/A	0	
7	Vibration (Variable-Frequency)	100~2000~100Hz 20G, 5min, 5Times, X,Y,Z	—	YES	10	N/A	0	For Discrete, others as applicable
8	Mechanial Shock (M/S)	1500G, 0.5ms 3 Times, X,Y,Z	—	YES	10	N/A	0	same as above
9	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	—	YES	10	N/A	0	same as above

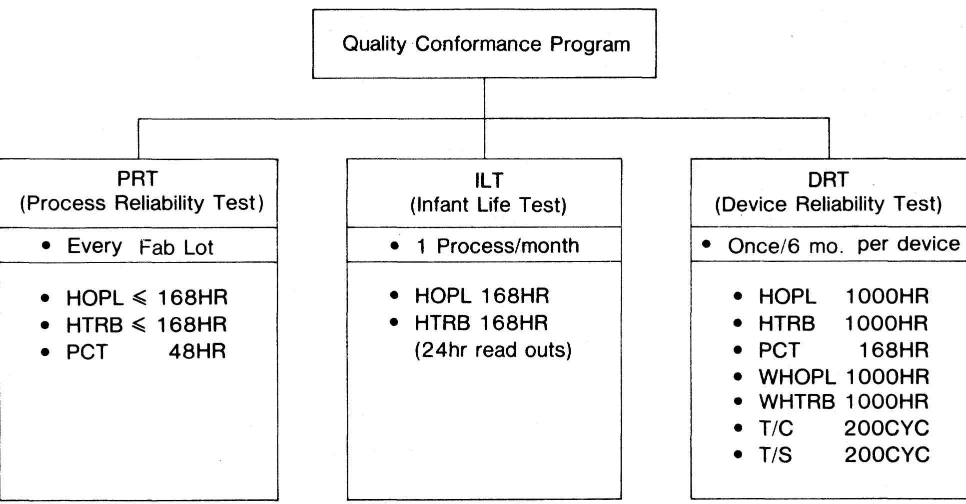
Note) • N/A: not available

4.5 Product Reliability (Quality Conformance) Monitors

Samsung implements periodic testing to monitor the ongoing reliability of its products. A subset of stresses used for qualification are run; they are seen as most critical for basic device reliability. Formally this is known as the Device Reliability Test System, or simply as DRT.

Lot-by-lot infant mortality reliability testing is also accomplished at Samsung. The purpose of this is to verify process integrity in a full QA step. Formally this is known as Process Reliability Testing, or more simply as PRT. Normally a short term accelerated lifetest and package reliability test are done, although exceptions are made in the case of special devices.

Although Samsung scrupulously utilizes statistical controls throughout it's production process, DRT and PRT serve as confirmation that indeed the customer does receive only high-grade units. The tables on the following give details of DRT and PRT processing.



Note: Test descriptions given on following pages.

Fig 10. Quality Conformance Program

(PRT/DRT Product Stress Methodologies)

1. PRT (Process Reliability Test)

Frequency: Every outgoing lot

No.	Test Item	Test Condition	Sample Size	LTPD	Accept. No.	Note
1	High Temperature Operating Life (HOPL)	Ta=Topr(max) $V_{CC}=V_{CC}$(max) 168HR max	45	10	1	for IC
2	High Temperature Reverse Bias (HTRB)	$Ta=T_j$(max) $V_{CB}=V_{CBO}\times0.8$ 168HR max	45	10	1	for Discrete
3	Pressure Cooker Test (PCT)	Ta=121°C±2°C 100% RH, 15PSIG 48HR	45	10	1	

2. ILT (Infant Life Test)

Frequency: 1 Process/month

No.	Test Item	Test Condition	Sample Size	Note
1	High Temperature Operating Life (HOPL)	$Ta=T_{opr}$(max) $V_{CC}=V_{CC}$(max) 168HR	300	24 Hr. Readouts (for IC)
2	High Temperature Reverse Bias (HTRB)	$Ta=T_j$(max) $V_{CB}=V_{CBO}\times0.8$ 168HR	300	for Discrete

3. DRT (Device Reliability Test)

No.	Test Item	Test Condition	Sample Size	LTPD*	Accept. No.	Note
1	High Temperature Operating Life (HOPL)	$Ta=T_{opr}$(max) $V_{CC}=V_{CC}$(max) 1000HRS	45	5 10	0 1	For IC
2	High Temperature Reverse Bias (HTRB)	$Ta=T_j$(max) $V_{CB}=V_{CBO}\times0.8$ 1000HRS	45	5 10	0 1	For Discrete
3	Pressure Cooker Test (PCT)	Ta=121°C±2°C RH=100%, 15PSIG 168HRS	45	5 10	0 1	
4	Wet High Temperature Reverse Bias (WHTRB)	Ta=85°C, RH=85% $V_{CB}=0.8\times V_{CBO}$ 1000HRS	45	5 10	0 1	For Discrete
5	Wet High Temperature Operating Life (WHOPL)	Ta=85°C, RH85% $V_{CC}=V_{CC(opr)}$ 1000HRS	45	5 10	0 1	For IC
6	Temperature Cycle (T/C)	−65°C↔25°C↔150°C 10min, 5min, 10min 200 Cycles	45	5 10	0 1	
7	Thermal Shock (T/S)	−65°C↔150°C(Liquid) 5min,<10sec, 5min 200 Cycles	45	5 10	0 1	

*LTPD 5: S Grade Units LTPD 10: A,B Grade Units.

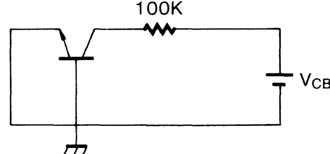
4.6 Reliability Tests

The tests run by the quality department are accelerated tests, serving to model "real world" applications through boosted temperatures, voltages, and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situations. These accelerated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions. Following are summaries of various stresses (and their conditions) run by Samsung on discrete and integrated devices.

High Temperature Operating Life ($V_{CC}=V_{CC}$(max), 125°C, Static or Dynamic)
High Temperature Operating Life is used to verify die integrity at high voltage and temperature conditions. Stabilities of die materials (oxide, metal, polysilicon etc.), construction (layout, architecture, process durability), and design are investigated.

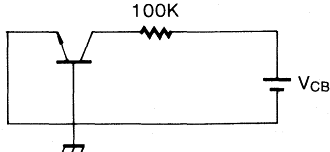
High Temperature Reverse Bias (80% max. BV_{CBO}, 150°C, static)
For this test, device integrity is checked through stressing of the main blocking junction at an elevated temperature and voltage. Overall product stability is investigated through leakage current monitoring; low leakage indicates good integrity.

High Temperature Reverse Bias (80% BV_{CBO}, 150°C)



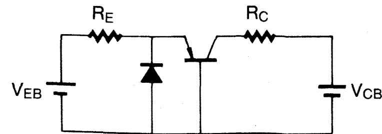
High Temperature Gate Bias (V_{GS}=20V, V_{DS}=0V, 150°C, static)
HTGB is utilized to analyze gate oxide and junction stability over extended periods of accelerated temperatures and voltages. This is crucial as it is used to establish integrity at a point of high device stress.

Wet High Temperature Reverse Bias (80% BV_{CBO}, 85% RH., Static)



Intermittent Operating Life (P_{MAX}, 25°C, 2 min on/2 min off)
This test is normally applied to scrutinize die bond thermal fatigue. A stressed device undergoes an "on" cycle, where there is thermal heating due to power dissipation, and an "off" cycle, where there is thermal cooling due to lack of inputted power. Die attach (between die and package) and bond attach (between wire and die) are the critical areas of concern.

Intermittent Operating Life (P= Pc_{max}, 25°C, 2 min on/2 min off)



Wet High Temperature Reverse Bias (80% max. BV_{CBO}, 85°C, 85% R.H., static) or (V_{CC}=V_{CC} (typ), 85°C, 85% R.H, static)
Wet High Temperature Reverse Bias Test is used to accelerate failure mechanisms by applying static bias on alternate pins at high temperature and humidity ambient (85°C/85°C R.H.). This test checks for resistance to moisture penetration by using an electrolytic principle to accelerate corrosive mechanisms.

Pressure Cooker Test (Unbiased, 121°C, 15 PSIG, 100% R.H.)
The Pressure Cooker Test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

High Temperature Storage (Unbiased, 150°C)
High Temperature Storage is utilized to test for both package and die weaknesses. For example, sensitivities to ionic contamination and bond integrity are closely scrutinized.

Temperature Cycling (Unbiased, −65°C to +150°C, air)
This stress uses a chamber with alternating temperatures of −65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

Thermal Shock (Unbiased, −65°C to +150°C, liquid)
This stress uses a chamber with alternating temperatures of −65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

Resistance to Solder Heat (Unbiased, 260°C, 10 sec)
Solder Heat Resistance is performed to establish that devices can withstand the thermal effects of solder dip, soldering iron, or solder wave operations.

Mechanical Shock (Unbiased, 1500g, Pulse=0.5msec)
This test determines the suitability of a device to be used in equipment where mechanical "shocks" may occur. Such shocks result from sudden or abrupt changes produced by rough (non-standard) handling, transportation, or field operations.

Variable Frequency Vibration (Unbiased, Range=100 to 2000 Hz)
Variable Frequency Vibration is done to model the effects of differential vibration in the specified range. Die attach and bonding integrity are particularly stressed, testing the mechanical soundness of device packaging.

Constant Acceleration (Unbiased, 10kg to 20kg)
This is an accelerated test designed to indicate types or modes of structural and mechanical weaknesses not necessarily detectable in Mechanical Shock and Variable Frequency Vibration stressing.

4.7 Relative Stress Comparisons

Many stresses are run at Samsung on many different devices. Through both theoretical and actual results, it was clearly determined which stresses were most effective. Also established were the stresses which weren't fully effective.

Comparisons have been made on the basis of defects able to be determined, efficiency in detection, and cost. For the reader's benefit, Samsung provides the results of its conclusions on the following pages.

Comparison of Reliability Test Methods

Test Method	Defect	Effectiveness	Cost	Remarks
Internal Visual Inspection	Lead Structure Metallization Oxide Film Foreign Particles Die Bond Wire Bond Contamination Corroded Substrate	Good	Slightly Inexpensive to Moderate	This method of screening must be performed for high reliability devices. Cost is affected by the degree of visual inspection
Infrared ray	Design(thermal)	Very Good	Expensive	For use in design evaluation only
Radiography	Die Bond Lead Structure(Gold) Foreign Particles Manufacturing (Gross Error) Seal Package Contamination	Extremely Good Good Good Good Good Good Good Good	Moderate	Advantage to using this screening method lies in the ability to test die frame/ header bonding, and to be able to perform inspection after sealing. However, some materials being transparent to X-rays (for example, Al and Si) are not able to be analyzed. The use of the complex test system results in cost six times that of visual inspection.
High Temperature Storage	Electrical stability Metallization Bulk Silicon Corrosion	Good	Very Inexpensive	This is a highly desirable screening method
Temperature Cycling	Package Seal Die Bond Wire Bond Cracked Substrate Thermal Mismatching	Good	Very Inexpensive	This screening method is one of the most effective for use
Thermal Shock	Package Seal Die Bond Wire Bond Cracked Substrate Thermal Mismatching	Good	Inexpensive	While this screening method is similar to temperature cycling, it enables high stress levels as well. It is probably equal to the temperature cycling method.
Constant Accelertion	Lead Structure Die Bond Wire Bond Cracked Substrate	Good	Moderate	Doubt exists as to the effectiveness of screening aluminum wires with stress levels in the range of 0~20,000 G
Shock (Without Monitoring)	Lead Structure	Fairly Poor	Moderate	Drop shock testing is thought to be inferior to constant acceleration methods. However, the pneupactor shock test is more effective. Shock test is a destructive test method.

4

Comparison of Reliability Test Methods (continued)

Test Method	Defect	Effectiveness	Cost	Remarks
Shock (With Monitoring)	Particles Intermittent Short Intermittent Open	Fairly Poor Fairly Good Fairly Good	Expensive	Visual inspection or radiography is more desirable for detection of particles
Vibration Fatigue	Lead Structure Package Die Bond Wire Bond Cracked Substrage	Fairly Poor	Expensive	This test is destructive and without merit.
Variable Frequency Vibration (Without Monitoring)	Package Die Bond Wire Bond Substrate	Fairly Poor	Expensive	
Variable Frequency Vibration (Without Monitoring)	Foreign Particles Lead Structure Intermittent Open	Fairly Good Good Good	Very Expensive	The effectiveness of the method for detecting particles depends on the type of particle
Random Vibration (Without Monitoring)	Package Die Bond Wire Bond Substrate	Good	Expensive	This screening method is more effective than variable frequency vibration(without monitoring), when used with equipment intended for space vehicle operation, although it is more expensive.
Random Vibration (With Monitoring)	Foreign Particle Lead Structure Intermittent Open	Fairly Good Good Good	Very Expensive	This is one of the most expensive screening methods
Vibrational Noise	Froeign Particles	Good	Expensive	
Radioisotope Leak Test	Package Seal	Good	Moderate	This screening method is effective for detecting leakage in the range 10E6~10E12 atm. ml/sec
Helium Leak Test	Package Seal	Good	Moderate	This screening method is effective for detecting leak in the range 10E6~10E12 atm. ml/sec
Gross Leak Test	Package Seal	Good	Inexpensive	Effectiveness is dependent upon volume. Testing is possible for detecting leaks above 10E-3 atm. ml/sec.
High Voltage Test	Oxide Film	Good	Inexpensive	Effectiveness Depends on Structure

Comparison of Reliability Test Methods (continued)

Test Method	Defect	Effectiveness	Cost	Remarks
Insulation Resistance	Lead Structure Metallization Contamination	Fairly Good	Inexpensive	
Intermittent Operation	Metallization Bulk Silicon Oxide Film Inversion/Channeling Design Parmeter Drift Contamination	Good	Expensive	Probably about the same as AC operating life
AC Operation	Metallization Bulk Silicon Oxide Film Inversion/Channeling Design Parmeter Drift Contamination	Very Good	Expensive	
DC Operation	Basically the Same as Intermittent Operation	Good	Expensive	The AC operation life method is more effective for any failure mechanism
High Temperature AC Operation	Same as AC Operation Life Test	Extremely Good	Very Expensive	Failures are accelerated by temperature. This is probably the most expensive and one of the most effective screening methods.
High Temperature Reverse Bias	Inversion /Channeling	Fairly Poor	Expensive	

4

4.8 Reliability Test Results

Extensive test results have been compiled through long term reliability monitoring (DRT) of devices. Current and historical data is entered into Samsung's Reliability Network, SRN. Thus, past performance of a device or it's family, assembly evaluation results, manufacturing change reliability results, etcetera, can all be seen via computer through SRN.

Results included in this manual are representative of products stressed, and contain data from the past year. Data is summarized from both die and package tests, on five critical stresses. Failure rates for long term life testing are in FITs, which are calculated using Arrhenius' Equation. (Arrhenius' Equation is summarized in the Appendix section). Samsung's failure rates are well below 50 FITs, which is acknowledged by customers and competitors alike as among the industry's elite.

1. Long Term Life Test Results

60% UCL, Ea=1eV

Family	Application	Steady State Operation Life: Ta=Topr max, $V_{CC}=V_{CC}(max)$ 1000 HRS			High Temperature Storage Life: Ta=125°C, 150°C 1000 HRS		
		Number of Samples	Number of Failures	Failure Rate (FIT)	Number of Samples	Number of Failures	Failure Rate (FIT)
T R	Small Signal	1228	4	8	430	2	14
	Power	1056	16	33	708	1	6
Bipolar I C	Op Amp	154	0	12	154	0	12
	Voltage Comparator	88	0	20	88	0	20
	Voltage Regulator	154	0	12	154	0	12
MOS I C	Calculator	44	0	41	44	0	41
	Watch	176	0	10	176	0	10
	Melody	132	0	14	132	0	14
MOS FET	N-Channel	1100	16	6	760	2	1

Note 1) FIT: Failure in time or failure unit; represents the number of failures expected per 10^9 (one billion) device hours (at 55°C).

2) TR: Transistor

2. Environmental Test Results

Family	Application	High Temp/High Humidity: 85°C, 85% R.H, V_{CC}(typ),			Pressure Cooker: 121°C, 100% RH, 168HRS			Thermal Shock: −65, 150°C, 200 Cyc. (liq)		
		Number of Samples	Number of Failures	Failure Rate (%/ 1KHRS)	Number of Samples	Number of Failures	Failure Rate (%/ 168HRS)	Number of Samples	Number of Failures	Failure Rate (%/ 200CYC)
T R	Small Signal	880	2	0.23	1020	12	1.2	1263	0	0
	Power	346	1	0.29	404	6	1.5	576	1	0.17
Bipolar I C	Op Amp	154	0	0	154	0	0	154	0	0
	Voltage Comparator	88	0	0	88	0	0	88	0	0
	Voltage Regulator	154	0	0	154	0	0	154	0	0
MOS I C	Calculator	44	0	0	44	0	0	44	0	0
	Watch	176	0	0	176	0	0	0176	0	0
	Melody	132	0	0	132	0	0	132	0	0
MOS FET	N-Channel	380	3	0.79	278	1	0.36	380	0	0

4.9 Product Outgoing Quality Levels

The quality of Samsung products reaching customers has improved steadily over the years. Nearly an order of magnitude reduction in outgoing product PPM levels has been achieved from 1983-7. Results can be seen below.

Average Outgoing Quality, or AOQ, is measured by the Quality Assurance Department. Prior to release, product is sampled according to MIL-STD 105D. Both electrical and visual/mechanical inspections occur. If inspection standards are met, product is approved for sales. Depending on the nature of the failure(s), rejected samples can cause an entire lot to be 100% tested and/or inspected, re-worked to screen out defective devices, or scrapped.

Electrical testing is typically done to product specification limits, guardbanded by a fixed percentage. Visual/mechanical inspection is performed to check for key package, marking, and lead parameters. (More extensive details are provided in Chapter 3, Assembly process control)

Although Samsung's AOQ levels are acceptable, efforts are constantly underway to reduce the figures (thereby increasing outgoing quality).
Enhanced focus on statistical process control in the manufacturing operation should help Samsung achieve it's goal of 50 PPM in 1988.

Samsung Product Electrical AOQ levels

(in PPM)

Product Family	1983	1984	1985	1986	1987	1988
Small-Signal Transistor	526	509	308	150	45	42
Power Transistor	968	1289	578	664	101	120
Linear-IC (Bipolar)	1669	1037	952	315	221	150
MOS-IC	—	—	2556	541	227	215

Samsung Product Visual/Mechanical AOQ Levels

(in PPM)

Product Family	1983	1984	1985	1986	1987	1988
Small-Signal Transistor	362	816	596	129	57	46
Power Transistor	452	1589	1297	796	140	95
Linear-IC (Bipolar)	709	782	391	140	77	63
MOS-IC	—	—	75	359	75	63

(PPM)

3000
2500
2000
1500
1000
500
0

'83 '84 '85 '86 '87 '88

(YEAR)

Note: Total = Electrical + Visual/Mechanical
S/S TR = Small Signal Transistor
PWR TR = Power Transistor
L-IC = Linear – IC

S/S TR
PWR TR
L—IC
MOS—IC

Fig 11. Total AOQ Levels

CHAPTER V DOCUMENT CONTROL SYSTEM

5.1 Introduction

Document control is a function wholly contained within the quality organization. As such, strict adherence to quality controls can be implemented and monitored within Samsung's manufacturing process by the quality department.

5.2 Policy

5.2.1 It is Samsung's policy that every process, material, piecepart, inspection, and test be documented in written specifications.

5.2.2 A "no spec, no work" policy is the powerful tool used to standardize production and achieve precision manufacturing.

5.2.3 Each specification is generated by an appropriate engineer, manager, or executive, and cannot be issued or changed without quality department approval.

5.2.4 Engineering Change Notifications, prevalent in any production environment striving to enhance product reliability, are an essential part of Samsung. Procedures for rapid implementation and customer notification (it appropriate) are built into the Document Control System.

5.3 Scope

5.3.1 The Document Control Group is responsible for the correct formatting, coding, typing, and dating of specifications to ensure they are properly signed, issued, and archived.
The group must also ensure that modifications are correctly raised, approved, recorded, issued, and archived.

5.3.2 Document Control established and maintains the standard audit program to attest that company policies (specifications) are carried out properly.

5.3.3 Along with quality control, appropriate (specified) parties are responsible for the technical contents of a given specification. They are also responsible for the timely introduction of technical changes.

5.3.4 Document Control ensures that all affected personnel are notified not later than two days after document recording. Supervision is appropriated to train relevant personnel in accordance with a written specification.

5.4 Document Flow

Flow is outlined in Figure 12 from document initiation to approval and circulation.

Appropriate Party

Specification Draft

(Committee of Inquiry)

Rejected

1.
2.

Approved

1.
2.

1. Drafts of Specification
2. Record of Committee.

(Approval; Higher than management level of authority)

Rejected

1.
2.

Approved

1.
2.

1. Drafts of Specification
2. Record of Committee.

Document Control Group

- Logging and Coding
- Formatting and Typing
- Copying
- Distribution
- Filing
- Auditing

Relevant Parties

- Circulation
- Training
- Filing
- Maintaining Security

Fig 12. Document Flow Chart

CHAPTER VI CUSTOMER RETURNS

6.1 General

Field quality information is an essential factor for improvement of product quality. Equally important, investigation of field failures and feedback of the results is required to service customers properly. This data can also serve as a direct guide to the improvement of reliability and quality for both Samsung and our customers.

6.2 Route & Action (refer to 6.3 for a flow chart summary)

6.2.1 Devices which have failed at the customer's site are returned through either customer or Samsung request. The sales department fills out a failure analysis request complete with pertinent data and a description of what the customer believes caused the problem. This request and the failed devices are forwarded to the quality control (Failure Analysis Group) department.

6.2.2 The quality Assurance and engineering departments investigate the characteristics of returned devices to determine the failure mechanism.
The results of the investigation are fed back to the user and appropriate manufacturing departments. If applicable, the detailed analysis is used to improve overall product reliability and quality.

6.2.3 The failure investigation has three main purposes. The first is to decide whether the devices are out of specification. The second is to analyze those devices which are out of specification to establish the cause of failure. This means to determine whether parts were destroyed by abuse or whether they had always been out of specification. The third purpose is to investigate any device fault to try and establish precisely how such a fault occurred. In this way corrective remedial action can be initiated to rectify customer abuse/misapplication problems. Every effort is then made to assist in eliminating such problems.

6.2.4 Each responsibility for claim settlment.

Department	Responsibility
Sales	1. Inquire, receive and relay claim. 2. Take first-aid measures on claim. 3. Settle a laim an delivery time and cost. 4. Make and transmit to Q.A dept. liaison form of claim received for quality claim. 5. Inform claim requester of settling result. 6. Investigate whether customer is satisfied with settling result. 7. Record and keep clam file. 8. Withdraw and resupply chaimed product.
Q.A	1. Make a plan for control and operation of claim. 2. Receive clain. 3. Survey trouble sources of claim and request its review to pertinent engineering dept. 4. Report the result of claim contents inquiry, and corrective actions. 5. Review and improve settling function of claim. 6. Promote activities to decrease claim. 7. Report regularly data compiled on claim settlement. 8. Conduct regularly futher checking for the products. 9. Record and keep claim file. 10. Supervise all the whole matters on claim.
Development (Design) Product Eng. Application Eng.	1. Investigate, analyze and notify the followings pursuant to corrective action details described in request form of claim countermeasure (1) Process history (4) Circuit Test (2) Production history (5) Other tests required. (3) Reproduciability Test
Production Production control	1. Implement instructions on counter-measures pursuand to result report of claim settlement. 2. Carry out retest, exchange and reproduction of claim products. 3. Inform Q.A Dept. of executed details.

6.3 Customer Return Procedure

Customer	Sales Dept.	Q.A. Dept.	Department Responsible for Corrective Action	Duration (Days)
Claim Occurence				
	Receive Claim	Receive Claim		
	Notification of Claim	Notification form of Claim (Form BQ0061#01)		D(0): Date when Q.A. Dept Receives Application and Samples
		Procure Information on Claim Occurence and Perform Failure Analysis		D+5: Finish Failure Analysis
	Finish Failure Analysis	Document Claim Counter Measure Suggestion (BQ0061 #02)	Distribute Request Form	
	Receive Analysis Result and Counter-Measure (BQ0061#02)		Review	D+10: Make and Notify Request form of Claim Countermeasure
		Notify	Complete Answer Form (BQ0061 #03)	D+17
Notify Countermeasure to Customer		Complete Claim Settlement After Verifying Execution of Countermeasure		
Finish			Take Action	

CHAPTER VII FAILURE ANALYSIS

7.1 Introduction

Semiconductor failure modes are diverse, caused by many different mechanisms. Some modes are due to defects, others to contamination, others to degradation phenomena, and others due to manufacturing operations themselves. Failure modes can also result from raw materials, processing, design errors, and incorrect device usage. Failure analysis of devices which have failed during testing, assessment, or in the field is an important tool in the continual program to enhance the quality of Samsung products.

7.2 Policy

Failure Analysis is known to be the backbone of product optimization. Definitive analyses and corrective actions are responsible for providing the highest quality product possible. Samsung gives full support to acquisition and upkeep of proper equipment, training, and engineering managment supervision of analyses. Samsung espouses a 2-week policy to provide analysis on customer returns.

7.3 Scope

All products are encompassed for the task of failure analysis. These products can result from qualifications, reliability monitors, or customer returns. Information is derived to enforce corrective actions (if necessary) and optimize production processes.

7.4 Procedure

A general failure analysis procedure is shown below. The method demonstrated in the flow chart applies to all rejects. However, each analysis is specific unto itself, so that a completely exhaustive analytical flow is impossible for the limits of this manual. Specific instances and examples of interest are provided later in the chapter. Also included in this section is a typical day-by-day accounting of a failure analysis in progress. A two-week turnaround is the objective, with greater than 90% of analyses lasting equal to or less than this duration. A sample analysis plan and report are attached at the conclusion of this section.

Identify Failed Sample

Identify Failure by Bench Tester and Computer

Determine Failure Mode

Parameter Failure

Identify Failed Area

Identify Circuit of Failed Area

Analyze Characteristics of Failed Area

Bake (Ion Contamination)

Retest / Restress

Decap/Visual Inspection

Function/Logic Failure

Identify Failed Block

Identify Failure by Bench Tester

Identify Circuit of Failed Area

Analyze Characteristics of Sensitivity on Test Parameter

Decap/Visual Inspection

Electrical Analysis by Dynamic Probing

Isolation for Parameter Analysis

Layer Strip/Visual Inspection/Cross-Section

Conclusion

Corrective Action

Fig 13. Failure Analysis Procedure Flow Chart

Applicable Comments for the above flow chart are made below.

7.4.1 **DETERMINATION OF FAILURE MODE**
The basic failure mode shall be determined with data from computer and bench testing. As a defect can represent various electrical failure modes, it is critical to determine the most basic failure mode. (For example, a V_{OL}/V_{OH} parameter failure may be also analyzed as a functional failure. However, it is very important to determino V_{OL}/V_{OH} as the basic failure mode.)

7.4.2 **IDENTIFICATION AND ANALYSIS OF FAILED CIRCUIT AREA**
Correlation shall be derived with general (macroscopic) failure phenomenon through circuit interpretation of the failed area.

7.4.3 **SENSITIVITY OF TEST**
Parametric value of failed sample shall be determined through adjusting DC and AC parameters, temperature range, etc.

7.4.4 **ION CONTAMINATION**
For a sample assumed to have an inversion phenomenon caused by ionic contamination, characteristics shall be identified by conducting a Ta=150°C, 24hour cure and repeating test/restress.
Contamination of a specific layer shall be determined by stripping each layer.

7.4.5 **DECAPSULATION**
There are 5 decap methods with respective merits and demerits. The appropriate method must be utilized on the basis of the characteristics and potential cause for each failure.

7.4.6 **ISOLATION AND DYNAMIC PROBING**
It is essential to isolate the probable failing part of the circuit for its electrical failure mode. Without isolation, exact detection of a failed part can not be accurately accomplished as an electrical failure mode has an influence on other parts of the circuit.

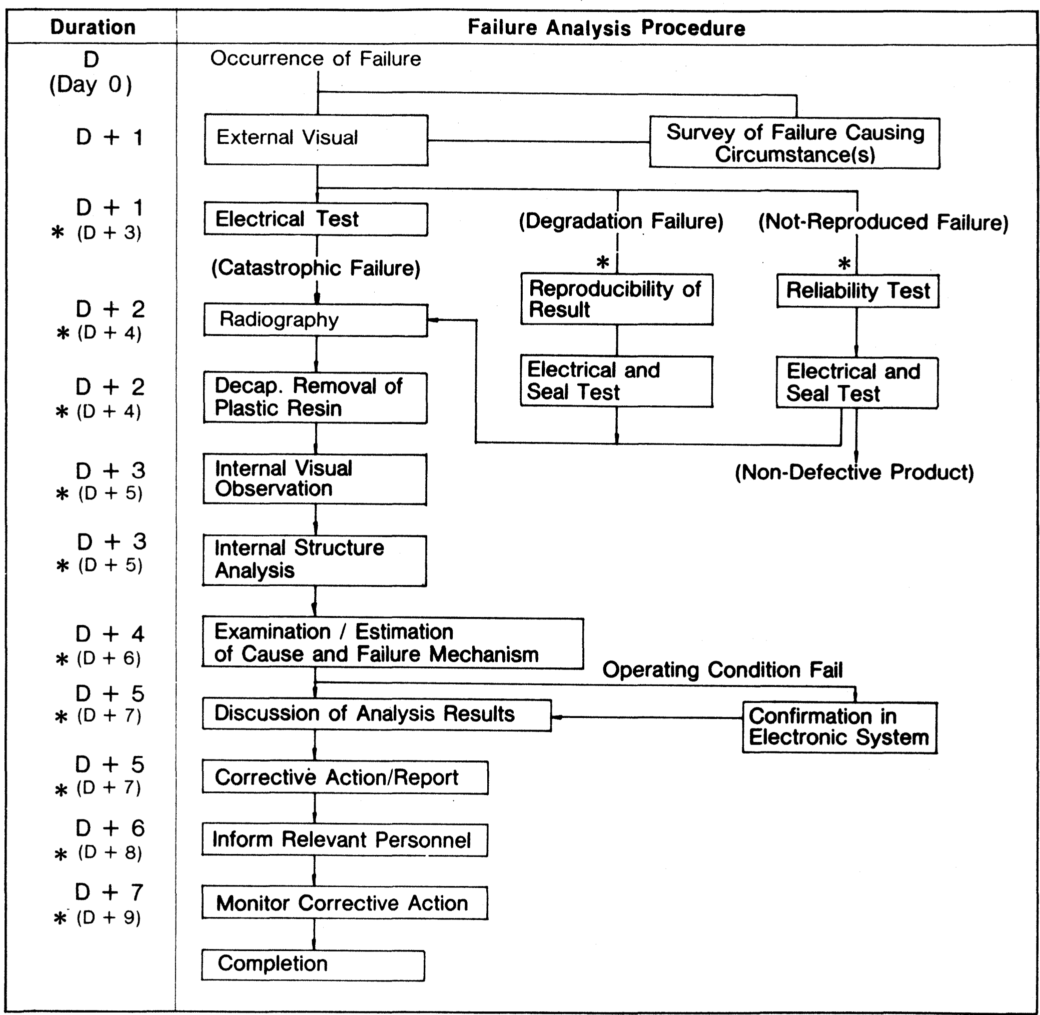
7.4.7 **LAYER STRIPPING**
Each layer strip should meet specification requirements with respect to time. It should never be the case that chemical attack is mistaken for causing the failure of a part.

7.4.8 **GENERATION OF ACTIVATION ENERGY**
Accelerated life testing requires generation of actual activation energies based upon establishing a definitive failure mode. This generation has a great effect in determining the acceleration factor of Arrehenius' model.

7.4.9 **CORRECTIVE ACTION**
Failure analysis is fully completed only by establishing a future plan and corrective action, which are taken to resolve a problem and prevent its recurrence.

FAILURE ANALYSIS

Procedure vs Duration of Failure Analysis



Document No: ____________________

Prepared by: ____________
Checked by: ____________
Approved by: ____________

Failure Analysis Plan

Date:

Receipt Date				Part No.			
Failure Status	Device History						
	Process			Run# (LOT#)			
Device Description	PKG Process			FAB Process		Pass'n Material	
	Function			Others			
Elec-trical Charac-teristic Review Result	Failure Mode						
	Probable Cause						
F/A Plan & Dates	Process Flow Chart & Dates				Available Equipment & Chemicals		
Conclusion					‡ Related Report		

Analysis Room Representative:

Fig 14. Failure Analysis Plan Format

7

Failure Analysis Table of Reliability Monitor Reject Mechanisms

Lot ID # ______________ Part No ______________ ROM Code ______________
Test Item ______________ Failure Q'ty ______________ Date ______________
Test Equipment ______________ Bin # ______________

Analysis Result Summary

1) Valid Failure					1) Invalid Failure				
#	Mech	Type	Location	Remark	#	Mech	Type	Location	Remark

‡ Table List

1. Valid Failure Mechanisms

0. Blank 1. Other
2. Defect Not Found
3. Analysis Not Performed
4. Charge Loss (Defect)
5. Charge Gain (Defect)
6. Contamination
7. Oxide Breakdown
8. Refresh Degrade
9. Silicon Defect
10. Surface Charge
11. Masking Defect
12. Contact Corrosion
13. Pyrox/Nitrox Hole
14. Line/Pad Corrosion
15. Line Corrosion
16. Pad Corrosion
17. Cracked Poly
18. Cracked Die
19. Cracked Pirox/Nitrox
20 Scratched Die
21. Micro-Cracks
22. Electromigration
23. Lifted Bond
24. Hermeticity
25. Charge Loss:int
26. Charge Loss:CC
27. Isolation
28. Metal Migration
29. Tin Bridging
30. Broken Wire
31. Chip-Crack
32. Analysis Pending
33. Die Off
34. Dendrite
35. Cracked Package
36. Leakage
37. Passivation
38. Bake Recovery
39. Oxidoner

2. Invalid Failure Mechanism

1. Pass
2. High Current Damage
3. Static Discharge
4. Die Charge/Package
5. Mixed Die
6. Wrong Product
7. Lost
8. Mistested
9. Other
10. Mis-Socketed
11. Missing Lead
12. Power Glitch

3. Type of Mechanisms

1. Blank
2. Other
3. Basic Function
4. Refresh
5. High Vcc
6. Low Vcc
7. Voltage Margin
8. Gross Leak
9. Fine Leak
10. DC:Other
11. DC:Open
12. DC:Short
13. DC:Power Supply Current
14. DC:Input Level
15. DC:Output Level
16. DC:Input Leakage
17. DC:Output Leakage
18. Speed Degradation
19. Corrosion
20. Dewetting
21. Pitting
22. Fuse Regrown
23. Analog Degrade
24. Visual
25. Electrical

4. Activation Energy (in eV)

1. Oxide Defect (0.3)
2. Silicon Defect (0.3)
3. Mask Defect (0.5)
4. Refresh (0.5)
5. Charge Loss/Gain (0.4)
6. Surface Charge (0.5-1)
7. Electromigration (1.0)
8. Slow Trapping (1.0)
9. Contamination (1.0-1.4)

5. Location

Failure Location is Related to Each Device's Layout

Fig 15. Failure Analysis Table

Document No:____________________

FAILURE ANALYSIS RESULT REPORT

APPROVAL	SUP	MGR	SMGR	ESDIR

Date:

Prepared by __________

item	Reliability Test Failure ( ), Claim ( ), Others ( )				
Failure Status					
Part No		ROM Code		S-Spec	
FPO #				Code	
Fab Lot #		Customer		FACR #	
Analysis Purpose	☐ Failure Analysis	☐	Correlation	☐ Others	

1. Failure Phenomenon

2. Analysis Result

3. Conclusion

4. Corrective Action

5. Distributed To

Fig 16. Failure Analysis Report Form

7.5 Failure Modes and Mechanisms

7.5.1 Failure mechanisms for devices vary widely.They are caused by both front-end (wafer) and back-end (assembly) processing. To classify problems and their instigations, the table listed below is provided.

Items and Causes of Failure Modes

Item	Type of Failure	Failure Mode	Cause
Wire Bonding	Wire Disconnection	Open	Incomplete Manufacture or Misuse
	Wire Short	Short	
	Purple Plague	Open, High Resistance	
	Bond Detaching	Open, High Resistance	
	Misplaced Bonding, Loose Contact	Open, High Resistance Short	Incomplete Manufacture
	Improper Bond Shape Erroneous Bonding	Open, High Resistance Open, High Resistance	
Junction Region	Destruction by Surge	Low Breakdown Voltage, Short, Open	Incomplete Manufacture or Misuse
	Hot Spot		
Case	Lead Disconnection	Open, High Resistance	Same as above
	Lead Short	Short, High Leakage	
Seal	Incomplete Seal	Breakdown Voltage Deterioration, High Leakage	Same as above
	Enclosed High Humidity Gas		
	Contamination of Surface		
	Dust and Dirt	Short, Low Breakdown Voltage Large Leakage	
Metallization	High Current Density	Open, Short	Misuse
	Electromigration	Open, High Resistance	
	Scratch	Open, Short	Incomplete Manufacture
	Insufficient Thickness Excessive Etching	Open, High Resistance	
	Contamination, Dust and Dirt	Open, High Resistance	Incomplete Manufacture or Misuse
	Poor Wiring and Element Connection		
Chip Mounting	Chip Crack	Open, Short	Same as above
	Chip Detaching	Open, Short, High Thermal Resistance	
Oxidized Film	Pinhole, Crack	Low Breakdown Voltage, Short	Incomplete Manufacture
	Insufficiently Oxidized Film Thickness	Low Breakdown Voltage	
Surface Treatment	Channel Formation	Low Breakdown Voltage High Leakage	Same as above
	Contamination		
Mask	Insufficient Photoresist	Low Breakdown Voltage	Same as above
	Mask Misaligment	Short, Open, High Leakage	
Material and Diffusion	Improper Impurity Density	Same as above	Same as above

7.5.2 Standard product reliability tests can naturally generate failures. In chapter 4, the tests are detailed. Here, in this section, a table is given which lists tests and their associated rejects. Each test has a specific purpose, and if there exists a particular product weakness, a given test will expose it. In this manner, by knowing a test and it's functions, a clear determination can be made as to the relevance of a failure for that particular test.

Reliability Tests and Associated Failure Modes

Item	Failure Cause / Test Condition	Diffusion	Oxide	Matalization	Wire Bonding	Package Environment	Package Seal	Lead Fatigue	Solderability	Mark	Die bonding
Item	Test Condition	• Contamination • Crystal Defect • Photoresist Reject	•Contamination • Pin Hole • Crack • Thickness Unstable	• Conpos. • Scratch • Void • Open	• interface • Corrosion • Mis-bonding • Wire Open • Chemical Interface	• Conductive ions • Inadequate Environments	• Sealing Reject	• Conpos.	• Marking	• Themal Reject	Resistance Reject • Crack • Chip Position Reject
T/C	−65°C→25°C→150°C 200 Cycles		0	0	0		0				0
T/S	−55°C→125°C 200 Cycles		0	0	0		0				0
Moisture Resistance	90-98%R.H./65℃3HRS 80-98%R.H./25℃8HRS 90-98%R.H./65℃3HRS 10 Cycles		0	0	0	0	0				
Vibration Fatigue	20G-3 Axis Orientation f=20 to 2000 cpe for 4 min. 4 cycles				0	0					0
Constant Acceleration	Pulse Duration: 0.1-1m sec Shock pulse: 0.5-3Kg				0						0
Mechanical Shock	1500g, 0.5ns Each Direction of X, Y and Z Axis				0						0
Lead Integrity	W=227g 90°C 3 times						0				
Marking	Isoprophylalcohol									0	
Solderability	Ta=230°C 5 Sec, Once With Flux								0		
Salt Spray	Ta=35°C, 5% NaCl				0				0		
OPL	Individual Spec	0	0	0	0	0					0
IOPL	Individual Spec	0	0	0	0	0					0
HTRB	Individual Spec	0	0	0	0	0					0
HTS	Individual Spec		0		0	0			0		
WHTS	80°C, 90%RH 85°C, 85%RH		0	0			0	0	0		
WHTRB	85°C, 85%RH Bias	0	0	0	0	0	0		0		0

Note: Test Conditions are further detailed in Chapter 4

7

7.5.3 An anomalous manufacturing step can manifest itself in many ways with respect to product reliability. The chart below depicts process steps, the types of rejects they can generate, and the way to defect such failures. Of course, there are numerous QC and Production checks along all stages of the manufacturing process. However, a semiconductor product typically involves so many operations it's nearly impossible to detect all potential reliability hazards. Thus, there are final electrical and visual tests, reliability tests, and statistical analyses which are run prior to product releasal. The chart below speaks to the electrical, visual, and reliability tests.

Failure Mechanisms of

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Wafer Fabrication	Dislocation and Stacking Fault	Degradation of Function Characteristics	Electrical Test Operation Life
	Non-Uniform Resistivity	Unpredictable Characteristic Values	Electrical Test
	Surface Abnormalities	Improper Electrical Characteristics, Short and Open	Electrical Test Operation Test
	Cracks, Chips, Scratches (Usually Caused During Handling)	Open and Short	Electrical Test Visual Inspection (Before Seal) Temperature Cycling
	Contamination	Degradation of Junction Characteristics	Visual Inspection(Before Seal), Temperature Cycling, High Temperature Storage, Reverse Bias
Passivation	Cracks and Pin Holes	Shorts, Low Breakdown Voltge	Temperature Cycling High Temperature Storage High-Voltage Test, Operation Life Visual Inspection (Before Seal)
	Non-Uniformity of Film Thickness	Low Breakdown Voltage Increase of Leakage Current in Oxide Film	Same as Above
Mask	Scratch, Crack, Scar of Photo Mask	Open, Short	Visual Inspection(Before Seal), Electrical Test
	Misalignment	Open, Short	Same as Above
	Abnormality of Photo-Resist Pattern (Line-Width, Space, Pin Hole)	Degradation of Characteristics Due to Parameter Drift Open, Short	Same as Above
Etching	Improper Elimination of Oxide Film	Open, Short, Intermittent Failure	Visual Inspection(Before Seal) Electrical Test Operation Life
	Under-Cut	Short or Open in Metallization	Visual Inspection (Before Seal) Electrical Test

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Etching	Spotting (Smear) Inhomogeneous Etching	Latent Short	Visual Inspection(Before Seal) Temperature Cycle, High Temperature Storage Operation Life
	Contamination (Photo Resist, Residue of Chemical Substance)	Low Breakdown Voltage Increase of Leak Current	Same as Above Reverse Bias
Diffusion	Improper Control of Doping Profile	Peformance Degradation Caused by Instability and Fault	High Temperature Storage Temperature Cycling Operation Life Electrical Test
Metallization	Scratched and Smeared Metallization (Caused During Handling)	Open and Short	Visual Inspection(Before Seal) Temperature Cycling Operation Life
	Thin Metallization Due to Insufficient Deposition or Oxide Film Step	Open or High Impedance Internal Connection	Electrical Test Operation Life Temperature Cycle
	Oxid Film Contamination Material Incompatibility	Open Matallization Caused by Poor Adhesion	High Temperature Storage Temperature Cycling Operation Life Test
	Corrosion(Residue of Chemical Substance)	Open Metallization	Visual Inspection(Before Seal), High Temperature Storage Temperature Cycle. Operation Life
	Displacement Contaminated Contact	High Contact Resistance, Open	Visual Inspection (Before Seal), Electrical Test, High Temperature Storage Temperature Cycle, Operation Life
	Improper Temperature and Period for Metallization	Peeled Metallization Poor Adhesion Short	Electrical Test High Temperature Storage Temperature Cycle Operation Life
Die Separation	Cracks and Chips Caused by Improper Dicing	Open	Visual Inspection(Before Seal) Temperature Cycling Thermal Shock Vibration Shock

7

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Die Bonding	Void Between Header and Die	Degradation Due to Overheating	Radiography, Operation Life Constant Acceleration Shock, Vibration
	Over-Spreading of Eutectic Solder	Short, Intermittent Short	Visual Inspection (Before Seal), Rediography, Vibration Shock
	Poor Bonding of Die to Header	Die Crack and Lifting	Visual Inspection (Before Sealing), Constant Acceleration, Shock, Vibration
	Mismatching of Materials	Crack or Peeling of Die	Temperature Cycling High Temperature Storage Constant Accelaration
Wire Bonding	Poor Bonding Strength	Open Wire, Open, Lifting Vibration Shock	Constant Acceleration
	Mismatched Material and Contaminated Bonding Pad	Lead Bond Peeling	Temperature Cycling High Temperature Storage Constant Acceleration Shock, Vibration
	Formation of Intermetalic Plague	Open Bonding	High temperature storage. Temperature Cycling. Constant Acceleration Shock, Vibration
	Insufficient Bonding Area or Spacing	Open Bonding Short	Operation Life Test, Constant Acceleration, Shock Vibration, Visual Inspection (Before Seal)
	Improper Bonding Arrangement	Open, Short	Visual Inspection(Before Seal) Electrical Test
	Die Cracks or Chips	Open, Shock	Visual Inspection (Before Seal) High Temperature Storage Temperature Cycling Constant Acceleration, Shock Vibration
	Excessive Loop or Sag in Wire	Short to the Case, Substrate or other Parts of the Leads	Visual Inspection(Before Seal), Radiography, Constant Acceleration, Vibration
	Crack, Scratch, or Scar on Lead	Wire Disconnection Causing Open, Short	Visual Inspection (Before Seal), Constant Acceleration, Shock Vibration

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
	Insufficent Elimination of Tail Wire	Short, Intermittent Short	Same as Above Radiography
Sealing	Incomplete Hermetic Seal	Performance Degradation, Shorts and Opens Caused by Chemical Corrosion and Moisture	Fine Leak, Gross Leak
	Bad Atmosphere in Package	Performance Degradation Due to Invesion Layer Channeling	Operation Life Reverse Bias, High Temp. Storage, Temperature Cycling
	Bending or Breaking of the External Lead	Open	Visual Inspection, Lead Fatigue
	Crack or Void in Seal Glass	Short or Open in Metalliza-tion Due to Leak	Seal, Electrical Test High Temperature Storage Temperature Cycling High Voltage Test
	Migration on Seal between Outer Lead and Metal Case	Intermittent Short	Low Voltage Test
	Electro-Conducting Particles Floating in Package	Same as Above	Constant Acceleration, Vibation Radiography
	Mismarking	Inoperable	Electrical Test

7.6 Equipment

A listing of important equipment used for failure analysis is shown below in tabular from. Samsung's committment to comprehensive analysis of all relevant rejects necessarily implies a usefulness for key analytical instruments. Constant efforts are made to both use and modify equipment to meet specialized investigations. However, only standard equipment, not a listing of hybrids (for confidential development purposes), is listed below.

1) Equipment for failure analysis

Category	Item	Application
Visual	1. Stereo Microscope	Use for visual inspection
	2. SEM (Scanning Electron Microscope)	Use to inspect the surface or cross-section of a device at high magnification. Through voltage contrast techniques, it is possible to analyze voltage levels while the device is operating
	3. Infrared Microscope	Using the infrared radiation emitted by a functioning device, a thermal map can be produced.
	4. X-Ray	Use to inspect the bonding wire of encapsulated devices.
	5. Metallugical Microscope	Inspect interconnects, contacts, bonds
	6. Radiographic Scope	Inspect bond wires, die attach
Elemental Analysis	1. Auger Electron Spectrometer (AES)	Used to detect and analyze contamination on the surface of a die
	2. EDAX Spectrometer	Used with SEM to analyze elements present in a device. This is done by measuring the energy distribution of X-rays produced by the interaction of primary electrons and the sample.
	3. Differential Interference Microscope	Used for elemental analysis
	4. Electron Probe Micro Analyzer (EPMA)	Used for current analysis

Equipment for failure analysis (continued)

Category	Item	Application
Elemental Analysis	5. Ion Micro Mass Analyzer (IMMA)	Spectral analysis of chemical constituents
	6. Surface Eveness Micrometer	Measures planarity
	7. Differential Scanning Calorimeter (DSC)	Permits the analysis of glasses and polymers-especially encapsulation resins-through the measurement of reaction heat
	8. Thermo Gravimetric Analyser	Used to determine the thermal stability of polymers and glasses by measuring variations in mass with temperature
	9. Plasma Etcher	Used to open devices encapsulated in epoxy resins, to remove silicon nitride, and to remove thin oxide films
Decapsulation System	1. Grinding Machines 2. Angle Lapping 3. Evaporation 4. Diamond Cutter (Cross Section Cutter) 5. Molding System 6. Jet-Etching System 7. Etching Solution 8. Hot Plates 9. Ventilation Hoods	Used to decapsulate devices, to cut the cross section of die, to remove a surface layer.
Electrical Test	1. Curve Tracer 2. TR, IC, MOS Tester 3. ESD Simulator 4. LCR Meter 5. DC-Analyzer 6. Noise Tester 7. Logic State Analyzer 8. Manipulator Probe System	Used to measure electrical characteristic of devices, to establish the cause of failure.
Stress Test	1. Temperature Probe System 2. Constant Temperature Oven 3. Oven for Oper Life Test 4. Humidity Oven 5. Vibration System	Used to stress or cure the failed devices to identify a failure mechanism. This is a very important tool for analyzing degradation phenomena and intermittent failures.

2) Methods and Equipment for Failure Analysis

Item	Contents of Inspection	Equipment for Analysis
External Visual Check	• Condition of Lead, Plating, Soldering, Welding Area • Mark, Date Code • Package damage • Solderability • Sealing	Stereo-Optical-Scope × 40 Optical Microscope × 100 Helium Leak Detector Gross Leak Detector (Using Fluorocarbon)
Electrical Test	• DC Parameter, AC Parameter Test • Function Test • Margin Test of Voltage and Temp. • Diode Characteristics between Each Pin • Disconnection, Short Circuit and / or Electrical Characteristic detected by the above Inspection	IC Tester Curve Tracer (HP4145) Oscilloscope DC Power Supply Oscillator (Sine Wave Pulse) Heat-Gun, Cooling Gas Spray Thermo-Spot
Radiography	• Internal Structure of Device is Checked Non-Destructively	Soft X-Ray
Decapping	• Internal Structure is observed after decapping	Metal Cutting Scissors, Nippers Cap opener, plastic etcher, Hot plate, Drill, HNO_3
Internal Visual Check	• Detection of Defective Spot on the Chip Surface • Detection of Discrepancy of Internal Connection (Metallization, Wire Bond -ing, Etc.) • Electrical Characteristics are Checked by Mechanical Prober • Detection of Hot Spot • Existence of Foreign Material	Optical Microscope Micro-Prober SEM Laser Cutter Infrared Micro Scanner Thermal Plotter Infrared Microscope
Internal Structure Analysis	• Cross Sectional Analysis of Chips to Observe Diffusion Layer of Oxide Film • Analysis of Metallic Elements • Removing of Over-Coating Glass and Aluminum Metallization	Optical Microscope SEM, MAX, AES, SAM, IMA Spectrometer Micro-Prober
Simulation Test	• Operational Test on Actual Equipment	Actual Electronic Equipment

7.7 General Information

7.7.1 In order to correctly and efficiently perform Failure Analysis, various prerequisites should be met. They are discussed below.

7.7.1.1 It is necessary to be knowledgeable about design and processing to accurately analyze failure mechanisms.

7.7.1.2 Adequate equipment must be available

7.7.1.3 Summarization of reliability stress conditions, field use conditions, failure rates, and other related information should be known.

7.7.1.4 Subsequent to failure events, failures must not be altered via additional stressing.

7.7.2 The chief failure mode among products returned from customers is overstress.
While the customer characterizes the failure mode as "catastrophic", "non-functional", "dead", etcetera..., the real mechanism is normally misuse of product. The customer, however, is not the cause of all failures. Samsung analysis does at times show vendor error. Examples are below.

7.7.2.1 In transistor junction regions, breakdown can be caused by current surges or hot spots. Externally applied overvoltages are the major failure cause.

7.7.2.2 For the connection between lead frame and chip itself, gold wire is routinely used. Exposure of products to conditions exceeding product ratings can result in failures such as opens and shorts. A brief tabular representation follows.

Package Connection Failures

Failure causes (Package)	**Mechanical Causes**	Excessive mechanical shock, incomplete bonding, defective pointed tools, inadequate wire shape
	Chemical Causes	Corrosion by contamination, formation of compounds among Al-Au metals (heat generation by current)
	Electrical Causes	Melting and fusing from excess current (Misuse or Surge)

7.7.2.3 Regarding packaging, the coexistence of moisture and an extremely small amount of impurities can cause rapid and serious failure

7.7.2.4 Aluminum metallization is frequently used to interconnect semiconductor elements. Failures related to this connection are, for example, scratches and current capacity shortages caused by an incomplete step portion of oxidization layers.
Substandard devices are removed by screening in the manufacturing process. However, devices exposed to conditions exceeding maximum ratings will fail in weak points in the metallization. Because the corrosion of aluminum traces is caused by the coexistence of moisture and an extremely small quantity of impurities, the use of plastic molded packages may cause troubles. This is especially true when the humidity is extremely high.

7.7.2.5 Other modes have been mentioned in detail in earlier parts of this chapter. The reader is invited to reference those sections for further information.

7.8 Customer Return Analysis

Samsung's objective is of course no returns at all, but that is very difficult given the myraid customer application situations. The goal for the coming year is to reduce fabrication and assembly defects each to less than five percent of all returns. This will be achieved through Statistical Process Control measures, along with effective test procedures.

NOTES

APPENDIX: RELIABILITY and RELIABILITY PROGRAM

Samsung manufactures semiconductor devices readily adaptable to a large number of applications ranging from consumer goods to communication and industrial systems. Continuing efforts are being made to produce high quality, highly reliable products so customers can use Samsung devices with confidence.
This appendix describe various aspects of semiconductor reliability and prediction theory.

1. Reliability of Semiconductor Devices

1.1 Definition

The definition of reliability assumes that the basic design of the device is adequate to provide the electrical performance required, and is able to withstand the electrical, mechanical and thermal stresses it will encounter in the application for the intended life of the equipment. Reliability is also used to show the probability that a device will operate within specified limits for a given time period and set of operating conditions.

Reliability, in general, can be explained with a "mortality (or bath-tub) curve". This curve indicate three different failure periods:
Initial failure period, random failure period, and wear out failure period, as shown in Fig. 17.
It is natural that equipment and components have decreased performance with longer and more frequent use. Although reliability depends greatly on the kinds of devices and the relationships between the type and degree of stress applied, failure can be roughly categorized into three modes as shown in Fig. 18.

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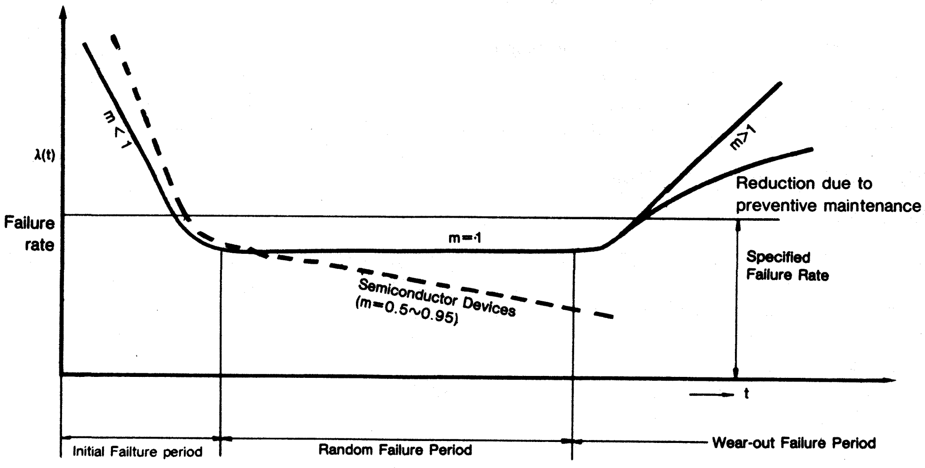

Fig 17. Failure Rate Curve (Bath-Tub Curve)

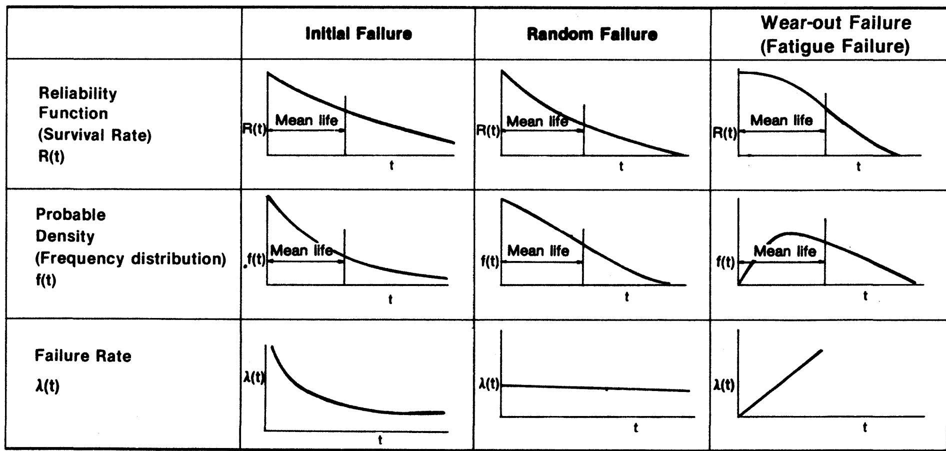

Fig 18. Failure Modes

1.2 Reliability Function

Reliability can be thought of as the probability that the system, equipment, and elements are operating normally. The following are necessary to express precise reliability.

1) To correctly define product function and failure
2) To define conditions of use and environmental factors
3) To express the failure rate as a function of reliability, probability of reliability, and non-reliability.
   Basic definitions allow the mathematical expression as follows:
   R(t): Reliability Function
   F(t): Non-Reliability Function
   $R(t) + F(t) = 1$

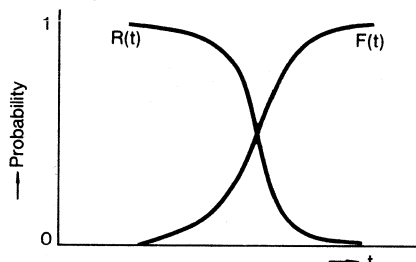

Fig. 18.1 Relation of reliability and non-reliability

From here, if f(t) is the probable failure density function

$$f(t)=\frac{dF(t)}{dt}=-\frac{dR(t)}{dt}$$

If $\lambda(t)$ is failure rate, then

$$\lambda(t)=\frac{f(t)}{R(t)}=\frac{-dR(t)/dt}{R(t)}=\frac{-dR(t)}{dt}\cdot\frac{1}{R(t)}$$

Reliability rate can be expressed with $\lambda(t)$ as

$$R(t)=\exp\left(-\int_0^t \lambda(t)dt\right)$$

The failure rate is expressed in %/1 KHR taking 1KHR as the unit of time according to MIL-STD.
(10^{-4}%/1 KHR = 1 FIT = 114,469 Years)

1.2.1 Probability Distribution for Reliability

— Continucus Distribution

1) Exponential distribution (constant failure rate)
   Exponential distribution is a random failure distribution. The non-reliability function and probability failure density function of it are as follows:

$$f(t)=\lambda e^{-\lambda t}(t\geqslant 0)$$
$$F(t)=1-e^{-\lambda t}$$

The failure rate is the constant (λ) in no relation to the time, the mean life μ is given as: $\mu=\frac{1}{\lambda}$

2) Logarithmic — normal distribution
   When ln t is adjusted by assuming a Normal-distibution, it result in a logarithmic normal distribution. The failure density function is:

$$f(t)=\frac{1}{\sqrt{2\pi}\cdot\sigma t}\exp\left\{-\frac{(\ln t-\mu)^2}{2\sigma^2}\right\}$$

3) Weibull distribution

The Weibull Distribution is generally recognized to be the most suitable as a reliability function for semiconductor devices. The reliability of semiconductor devices is expressed by the following factors of the Weibull Distribution.

Reliability Function: $R(t) = \exp\left\{ - \frac{(t-y)^m}{\eta} \right\}$

Cumulative distribution function: $F(t) = 1 - \exp\left\{ - \frac{(t-y)^m}{\eta} \right\}$

Probable density function: $f(t) = \frac{m}{\eta} \cdot (t-y)^{m-1} \cdot \exp\left\{ - \frac{(t-y)^m}{\eta} \right\}$

Instantaneous failure rate: $\lambda(t) = \frac{m}{\eta}(t - y)^{m-1}$

Mean life: $\mu = \eta^m \, \Gamma(1 + \frac{1}{m})$

* note 1) Here, $\Gamma(t)$ is the gamma function.

The relationship between m and $\Gamma(1 + \frac{1}{m})$ is shown in Fig.18.2

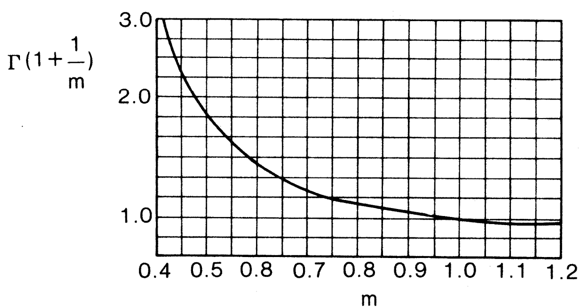

Fig. 18.2 Relationship between shape parameter m and gamma function

This distribution function includes location parameter y, scale parameter η, and shape parameter m.

The shape parameter can be utilized to determine the mode of each failure as follows.

- $m<1$ Initial failure
- $m=1$ Random failure (Exponential distribution)
- $m<1$ Wear-out failure

For checking whether the reliability function complies with the Weibull function or not, and obtaining the above parameters, y, η, and m, Weibull probability paper can be utilized.

4) Gamma Distribution
The Gamma distribution can be considered if and when the failure first occurs, for instance after m times of hazardous shocks are applied. h may be taken as the number hazardous shocks given in a unit of time.

$$f(t)=\frac{h^m}{\Gamma(m)}\cdot t^{m-1}\exp(-ht)$$

$$\lambda(t)=\frac{t^{m-1}.\exp(-ht)}{\int_t^{\infty}x^{m-1}.\exp(-hx)dx}$$

— Discrete Distribution

1) Geometric Distribution
The Geometric distribution is used to show the reliability.
The failure density function f(t) is

$$f(t)=p\cdot q^{t-1} \qquad (p+q=1)$$

In this case, P is the probability of failure occurrence during the time from (t-1) to the next time t.

2) Binomial Distribution
The Binomial distribution shortly described is the discret type of distributions mainly used for the sampling inspection.

$$P_B(t)=\binom{n}{t}P^t(1-P)^{n-t} \qquad (t=0,1,\ .....n)$$

3) Poisson Distribution
Assuming that $np=\lambda$ (Binomial Distribution)
If $n\rightarrow\infty$ and $P\rightarrow 0$, the binomial distribution becomes the poisson distribution.

$$P_B(t)=\frac{\lambda^t}{t!}\cdot e^{-\lambda}$$

where the parameter λ is equivalent to np in the binomial distribution.

1.2.2 Measure to express reliability, failure rate and reliability index.

1) Failure rate is defind as "the rate that a system, equipment, and devices (such as semiconductor devices), which have been in operation would develop failures per unit time." If the reliability function is denoted as R(t), the failure rate which is also a function of time can be expressed as:

$$\lambda(t)=-\frac{dR(t)}{dt}\cdot\frac{1}{R(t)}$$

In general there are 2 kinds of failure rates: Instantaneous failure rates and mean rates. "Failure Rates" in a simple statment often refers to the instantneous failure rate. The failure rate (t) in this section also means the same. A mean failure rate $\overline{\lambda}(t)$ can be obtained from the following fomula:

$$\overline{\lambda}(t)=\frac{\text{Total number of failures in a certain period}}{\text{Total operating hours}}=\frac{n}{\Sigma\, tj\, nj+(n_o-n)t}$$

Where nj is the number of failures at time tj, n is the number of failures in the observation period t, and n_o is the number of devices on test or operating. When n_o is sufficiently large, the mean failure rate can be expressed as follows:

$$\overline{\lambda}(t)=\frac{1-R\,(t)}{\int_0^t t.f(t)dt+t.R(t)}=\frac{1-R(t)}{R(t)dt}$$

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Where f(t) is the probability density function. However, the instantaneous failure rate $\lambda(t)$ and mean failure rate $\lambda(t)$ as defined above cannot easily be obtained from test results or practical data. Therefore, the following formula has been used conventionally as the measure of failure rates:

$$RI(t) = \frac{1}{R(o)} \cdot \frac{1 - R(t)}{t} = \frac{n}{no \times t}$$

This expression is quite pratical, such that the approximate number of failures in a certain period, and thus the approximate reliability, can be estimated instantly. Here, R(t) is called the reliability index, and should be distinguished from $\lambda(t)$ and $\lambda(t)$

If it is proven that R(tj) is 99% in a certain period of time tj, the mean failure rate after tj can be estimated as shown in Fig. 19(a), the reliability index after tj as shown in Fig. 19(b), and the instantaneous failure rate after tj as shown in Fig. 19(c).

The following should be taken into account:

A) Reliability index RI(t) may frequently be accompanied by some error when it is used as a direct means to calculate the instantaneous failure rate $\lambda(t)$ and mean failure rate $\lambda(t)$. Such an error would become greater as the value of m deviated more from 1.0.

B) If m = 1.0, the reliability function is determined by an exponential distribution, and the failure rate is said to be constant, regardless of time.
However, this applies only to instantaneous and mean failure rates, but not to the reliability index.

1.3 Reliability of Equipment

With recent advances in electronics, electronic equipment has become more complicated in composition. Suppose some equipment has no semiconductor devices and is used under the condition that its t-hour-later reliability will be λ(t). Then, the reliability R(t) of this "machine" based on the failure of devices can be obtained from the following equation:

$$R(t) = \{r(t)\}^{n_o}$$

However,

$$r(t) = \exp\left\{-\left(\frac{t}{\eta}\right)^m\right\} = \exp\left(-\frac{\lambda(t)\cdot t}{m}\right)$$

Therefore,

$$R(t) = \exp\left\{-\frac{\lambda(t)\cdot t}{m}\right\}^{no} = \exp\left(-\frac{no\cdot\lambda(t)\cdot t}{m}\right)$$

And furthermore, can be approximated as:

$$R(t) = 1 - \frac{n_o\,\lambda(t).t}{m}$$

As seen from these equations, as more components are employed in a piece of equipment, careful consideration should be given to the selection and use of them. In considering the reliability of equipment, a measure called MTBF (mean time between failures) is often used. MTBF is the average operation time between failures. The MTBF of the above-mentioned equipment, which has n_o semiconductor devices, and is used under the condition that its t-hour-later instantaneous failure rate will be λ(t) (based on the failure of its semiconductor devices), is as follows:

$$MTBF = \frac{m}{n_o\lambda(t)}\,\Gamma\left(1 + \frac{1}{m}\right) \quad (\Gamma\text{: Gamma function})$$

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1.4 Failures of Semiconductor Devices

Conventionally, the failure rates of electronic components and those of systems and equipment which incorporate these components are often indicated by a bath-tub curve. However, semiconductor devices may provide the shape parameter m, which is smaller than 1 (i.e 0.5 to 0.95 usually). If the stress conditions applied are not specific, the failure of these devices may be classified into initial failures, with a curve different from the bath-tub curve. That is, semiconductor devices would have a longer initial failure time, more than 6 months in many cases, as the transition from initial failure period to random failure period is not always distinct.

For reliability to be estimted after t=tj when R(t)=99%, it is a function of the value of shape parameter "m" as shown in Fig. 20. Thus, semiconductor devices have a far longer life than other equipment belonging to an exponenitial distribution (m=1). In other words, semiconductor devices, which can be used without failure for lengthy period of time, have longer reliability relative to other system components, so that regular replacement for maintenance will be detrimental for the reliability of the equipment.

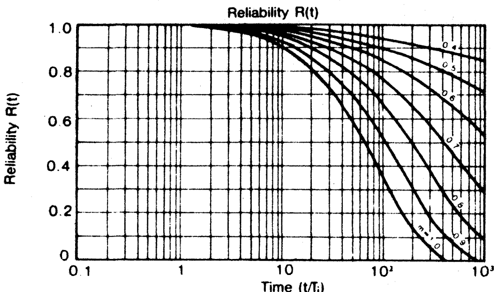


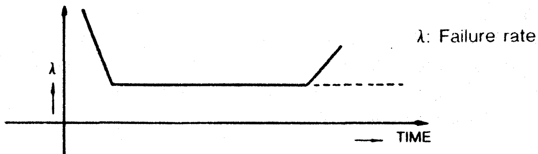
Fig. 20. Reliability to be estimated after t=Tj when R(t)=0.99 was recognized.

2. Accelerated Reliability Testing

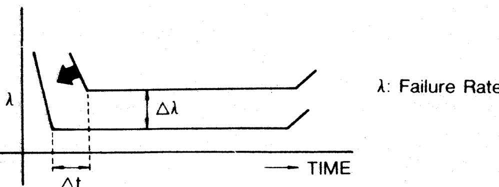
There are two types of reliability tests: those performed during design and development, and those carried out in production. The first type is usually performed on a small sample, but for long periods or under very accelerated conditions to investigate wearout failures and determine tolerances of design. The latter type of tests is performed periodically during production to check, maintain, and improve the assured quality and reliability levels. All reliability tests performed by Samsung are under conditions more severe than those encountered in the field. The conditions, although accelerated, are chosen to simulate stresses that devices will be subjected to in actual operation. Care is taken to ensure that the failure modes and mechanisms are unchanged.

2.1 Fundamentals

A semiconductor device is very dependant on its conditions of use (e.g. junction temperature, ambient temperature, voltage, current, etc.) Therefore, to predict failure rates, accelerated reliability testing is generally used. In accelerated testing, special stress conditions are considered as parameters related to failure modes. Actual operating life time is predicted using this method. Through accelerated stresses, component failure rates are ascertained, in terms of how many devices (in percent) are expected to fail every 1000 hours of operation. A failure rate vs time of activity graph is shown below (the so-called "bathtub curve")



During the initial time period, products are affected by the "infant mortality" intrinsic to all semiconductor technologies. End users are very sensitive to this parameter, which causes early assembly/operation failures of their system. Samsung periodically reviews and publishes life time results. At this time a new set of failure rate targets are being defined. These targets are being translated into actual required test hours. The goal is a steady shift of the limits as shown below.



2.2 Accelerated Humidity Tests

To evaluate the reliability of products assembled in plastic packages, Samsung performs accelerated humidity stressing, such as the pressure cooker test (PCT) and wet high temperature life test (WHOPL).

Fig. 21. Shown below are results obtained with these tests, which illustrate the improvements in recently years. These improvements result mainly from the introduction of purer molding resins, new process methods, and improved cleanliness.

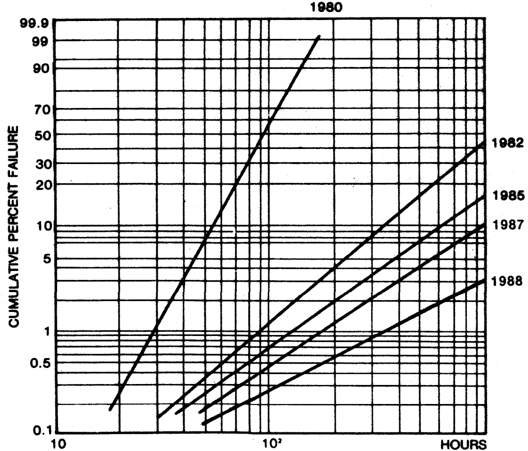


Fig 21. Improvement in humdity tests during recent years.

1) Calculation of Acceleration Factor
The acceleration factor for humidity stressing can be calculated from:
$AH = \exp\{4.4 \times 10^{-4} [(RH)^2_s - (RH)^2_0] + 6.9 \times 10^3 [1/T_o - 1/T_s]\}$,
where the subscripts S and 0 refer to the stress and operational environments, respectively. RH is in percent and T in ° K. The equation is for use over the humidity range 30% to 90% RH; below 30% RH, moisture induced failures are not expected, and at 100% RH, as used in pressure pot test, the equation has not been validated.

2.3 Accelerated Temperature Tests

Accelerated temperature tests are carried out at temperatures in the range of 75°C to 200°C for up to 6500 hours.
These tests allow Samsung to evaluate reliability rapidly and economically, as failure rates are strongly dependent on temperature.
The validity of these tests is demonstrated by the good correspondence between data collected in the field and laboratory results obtained using the Arrhenius model. Fig. 22 shows the relationship between failure rates and temperature obtained with this model.

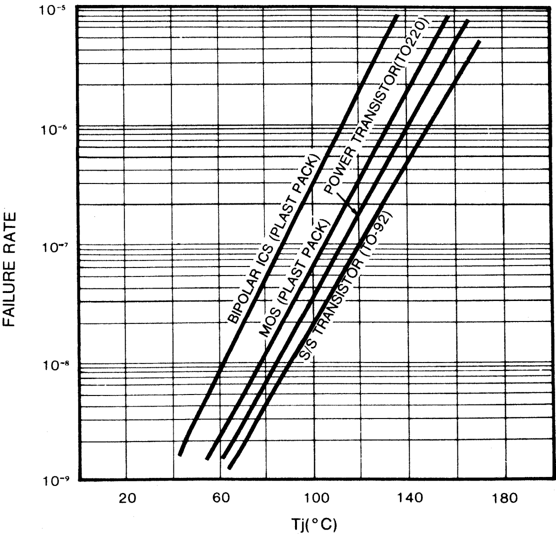


Fig 22. Failure rate vs. temperature

2) Activation Energy Estimate
Clearly the choice of an appropriate activation energy, Ea, is of paramount importance. The different mechanisms which could lead to circuit failure are characterized by specific activation energies, whose values are published in the literature. The Arrhenius Equation describes the rate of many processes responsible for the degradation and failure of electronic components. It follows that the transition of an item from an initially stable condition to a defined degraded state occurs by a thermally activated mechanism. The time for the transition is given by an equation of the form:

$$MTBF = B \exp(Ea/KT)$$

$$\left\{ \begin{array}{ll} MTBF & = \text{Mean time between failures} \\ B & = \text{Temperature} - \text{Independent constant} \end{array} \right\}$$

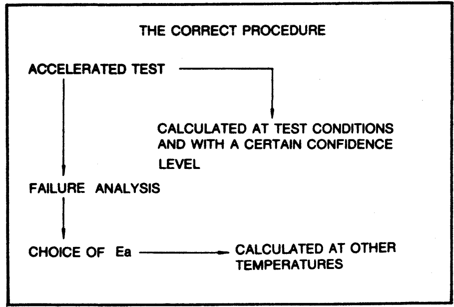
MTBF can be defined as the time to suffer device degradation. The dramatic effect of the choice of the Ea value can be seen by plotting the MTBF equation. The acceleration effect of a 125°C device junction test with respect to 70°C actual device junction operation is equal to 107 × for Ea=1 eV and 4× for Ea=0.3 eV.
Some words of caution are needed about published values of Ea:

A) They are often related to high temp-tests where a single Ea (with high value) mechanism has become dominant.
B) They are specifically related to the devices produced by that supplier (and to its technology), for a given period of time.
C) They could be modified by the mutual action of other stresses (voltage, mechanical, etc.)
D) Field device – application conditions should be considered.

(Activation Energy for Each Failure Mode)

Failure Mechanism	Ea
Contamination	1~1.4 eV
Polarization	1 eV
Aluminum Migration	0.5 eV
Trapping	1 eV
Oxide Breakdown	0.3 eV
Silicon Defects	0.5 eV

Fig 23. LIFE HOURS



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3) Failure rate evaluation

Accelerated testing defines the failure rate of the products. By derating the data at different conditions, the life expectancy at the actual operating conditions can be predicted. In its simplest form, the failure rate (at a given temperature) is:

$$F.R. = \frac{N}{D.H}$$

Where, N=number of failures
D=number of components
H=number of testing hours

If we intend to determine the F.R. at different temperatures, an acceleration factor must be considered. Some failure modes are accelerated by temperature stressing based on the accelerations of the Arrhenius law.

$$F.R. = A \exp (Ea/KTj)$$

F.R.= Failure Rate
A= Constant
Ea= Activation energy for the failure mechanism
K= Boltzman's constant
Tj= Absolute junction temperature

For two different temperatures

$$F.R.(T1) = F.R.(T2) \exp\left\{\frac{Ea}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right\}$$

F.R.(T1) is a point estimate, but to evaluate this data for an interval estimate, we generally use χ^2 (CHI square) distribution. The example follows;

Unit:%/1000HR

Device-Hours at 125°C	Fail	Failure Rate at 60% Confidence Level			
		Point Estimate	90°C	70°C	55°C
1.7×10^6	2	0.18	0.0108	0.0017	0.0004

The activation energy, from analysis, was chosen as 1.0 eV, based on test results. The failure rate at the lower operating temperature can be extrapolated by an Arrhenius plot.

2.5 Test circuits for accelerated testing

Test Item	Condition
Operation Life Test (Diode)	V_{AC} max<V_R V_{AC} max = V_R max (50 or 60Hz) $^{+10}_{-5}$% R_L=V_{AC}(Peak)/ I_F(Peak) Ta=25±5°C, 1000 Hr
Operation Life Test (Voltage Regulator)	P_c=P_c max ±5% T_a=25±5°C, 1000 Hr Voltage drop at R_L is more than V_E
High Temperature Reverse Bias Test (Diode)	V<V_R max ±5% T_a=T_j max, 1000 Hr
Operation Life Test (Transistor)	V_C=0.4 – 0.6×V_{ceo} max I_E is designed to P_C=P_C max Or T_j max V_C, I_E tolerance is ±5% T_a=25°C, 1000 Hr * To protect against oscillation, it is recommended to use 0.01 uF capacitor in E-B, C-B, C-E.
Operation Life Test (FET)	V_{DS}=0.4~0.6×V_{DS} max. I_D, P_T are determined at P_T=P_T max. V_{DS}, I_D tolerance is ±5% T_a=25°C, 1000 Hr * During test, if the gate is shorted, the device is destroyed by overcurrent
Intermittent Operation Life Test (TR, FET)	* Test circuit is equal to operating life test circuit. ON/OFF time is determined by individual specification.

2.5 Test circuits for accelerated testing (continued)

Test Item	Condition
High Temperature Reverse Bias (Transistor)	Short, V_C, V_{CC} $V_C=0.7\sim0.8\times V_{cbo}$ max. V_C tolerance is ±5% $T_a<T_j$ max, 1000 Hr * If leakage current produces heat, $T_a \leq T_j$ max should be maintained by reducing T_a or V_{cc}
High Temperature Ring (IC)	V_{CC} (gates 1, 2, ..., N) 1. Inverter Gate Ring Oscillation N: Odd 2. Non-Inverter Gate Ring Oscillation N: Even Ta: Topr. max 1000 Hr ex) Bipolar Gate Circuit MOS Gate Circuit
High Temperature Operating Life Test (IC) (Dynamic)	V_{cc}, in (gates 1, 2, 3, ..., N) Input: specified input pulse T_a: Topr. max 1000 Hr ex) Bipolar Gate Circuit, MOS Gate Circuit, Flip-Flop Circuit, Bipolar Memory
High Temperature Operating Life Test (IC) (Static)	1. Voltage is supplied to V_{CC} and therefore output states are H or L ex) Bipolar Gate Circuit, Flip-Flop Circuit, MOS Gate, MOS Memory 2. Voltage is supplied to V_{CC} and Input, therefore special bits are read ex) Bipolar memory 3. Voltage is supplied to V_{CC}, Input is GND and output is open ex) Comparator, Arithmetic Amplifier

3. Use of Semiconductor Devices to Maintain Reliability

Semiconductor reliability is dependent on a manufacturer's process factors, as well as a user's circuit design and environmental conditions. Therefore, Pc max, derating, and handling methods which are the responsibility of the user, are described in this section.

3.1 Absolute Maximum Rating

Absolute maximum ratings of voltage, current, power, and temperature are specified for semiconductor devices. If any of these are exceeded, degradation or destruction of the device may occur. Transients or slight violations of maximum ratings may cause device degradation resulting in gradual failure and longer term reliability problems. Steady state or large violations of maximum ratings can result in short term or even instantaneous device failures. Voltage, current, power, and temperature are all related, and care must be taken such that operation at the allowable specification limits of one parameter does not cause violation of the allowable limits of related parameters.

1) Maximum Rating for Transistors and Diodes.
   A. Voltage Rating
      1. Diodes
         a. Peak reverse voltage (VRM)
            Peak voltage that may be supplied with reverse polarity. This is limited to avalanche breakdown voltage.
         b. D.C. reverse voltage (VR)
            Reverse voltage that can be supplied continuously (may be limited by inverse leakage current.)
      2. Transistors
         a. Collector-base voltage (VCBO)
            Collector-base voltage characteristics are the same as a diode.
            Thus, when C-B is reverse biased, a small leakage current (ICBO) flows.
            When the C-B reverse voltage is increased continuously, the junction depletion layer also increases. A density of 10V/cm can be approached, whereby current is greatly enhanced.
            This is known as an avalanche phenomenon.
            Using the avalanche multiplication factor "M", the following equation is applicable to junction transistors:

$$M = \frac{1}{1 - (VCB/VB)^m}$$

VCB = PN junction voltage
VB = Electron avalanche breakdown voltage
M = Experimetal constant, with values listed below

Material	N Type	P Type
Ge	m=3	m=6
Si	m=4	m=8

Note: VCB is determined by VCBO and VB by diffusion density.

b. Emitter – Base voltage (VEBO)
   Determined by E-B junction avalanche or zener breakdown
c. Collector – emitter voltage (VCEO)
   Determined by VCBO and HFE

$$VCEO = \frac{1}{\sqrt[m]{1 + hfe}} \cdot VCBO$$

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d. Collector – emitter voltage (VCER)
This is the C-E reverse breakdown voltage. In this situation, C-E is connected by a resistor and determined by:

$$VCER = VCBO \cdot \sqrt[m]{1 - \frac{ICBO\ (rb + RBE)}{VTF}}$$

VTF = Base – emitter forward threshold voltage: 0.7V for Si

e. Collector – emitter voltage (VCES)
When E-B is a short, C-E reverse breakdown voltage is determined by:

$$VCES = VCBO \cdot \sqrt[m]{1 - \frac{ICBO \cdot rb}{VTF}} \approx VCBO$$

f. Collector – emitter voltage (VCEX)
When E-B is reverse biased by a resistor, C-E reverse breakdown voltage is determined by:

$$VCEX = VCBO \cdot \sqrt[m]{1 - \frac{ICBO\ (rb + RBE)}{VTF + VBB}}$$

g. Collector – emitter votage (VCEV)
When B-E is reverse biased, C-E reverse breakdown voltage is determined by:

$$VCEV = VCBO \cdot \sqrt[m]{1 - \frac{ICBO \cdot rb}{VTF + VBB}} \approx VCBO$$

Generally, this is expressed as VCEX.

h. The relationship these rating is, generally,
$VCBO \approx VCEV \approx VCES > VCER > VCEO$. This is shown in Fig. 24 below.

B. Current Rating.

(1) Diodes

a. Peak forward current (I_{FM}). Limited by the power rating. Current up to this value may be repeatedly passed through the device.

b. Average forward current (Io). The average value of the forward current, when an AC wave is rectified. DC current of this value may be passed continuously.

c. Surge Current (I_{FS})
The current that may be instantaneously input within a specified time.

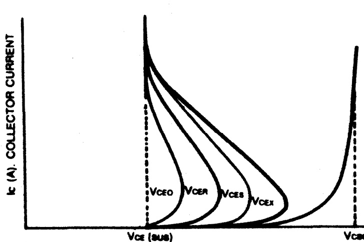

Fig. 24 Relationship of Collector BV Voltage

(2) Transistor

a. Collector Current (I_C)
It is generally limited at the point where HFE reduce to 50% of max HFE.
If it is not over the power rating, this current can be steady state. Generally this current is not limited. For small signal transistors:
($I_C \leqslant IA$):$I_B \leqslant I_C$; For power transistors: $I_C > IA$)

(3) Temperature Rating

This is determined by basis semiconductor package materials. The T_j max relationship is described below:

Material	T_j max	Ramark
Ge	75 ~ 90 °C	
Si	100 ~ 150°C	Surface stabilization type
Planar - Si	150 ~ 200°C	

The relationship between average life(Lm) and Tj(°K) is:

$$\text{Log Lm} = A + \frac{B}{Tj}$$ (A,B are intrinsic constants for transistors)

C. Power Rating

(1) Diode power rating is generally not specified. However, power consumed occurs mainly during the forward biased condition. Therefore, if forward current is specified, the power rating can be specified.

(2) Transistor
Pc(Collector consumed power) or Pt(Total power dissipation: sum of collector and emitter power dissipation) are specified at an ambient temperature of 25°C (free air), and case temperature of 25°C (with an infinitely large heat sink).

$$Pc = \frac{Tj\text{-}Ta}{R_{th(j\text{-}a)}}$$ (Free Air)

$$P_t = \frac{Tj\text{-}Tc}{R_{th(j\text{-}a)}}$$ (With an infinite large heat sink)

Ta = Ambient temperature (generally 25°C)
Tc = Case temperature (generally 25°C)
$R_{th(j\text{-}a)}$ = Thermal resistance from junction to ambient
$R_{th(j\text{-}c)}$ = Thermal resistance from junction to case

2) Maximum Rating for ICs
The maximum rating for an IC is specified by the following parameters. The maxima must not be exceeded or damage to the device may result.

a. V_{CC} or V_{DC}
This is the maximum voltage that can be supplied between power pin and ground. The voltage rating is related to the internal transistors' breakdown voltage.
b. Input Voltage Rating (Vin)
This is the maximum emitter breakdown voltage of the input transistor or input diode.
c. Output Voltage Rating (Vout)
Maximum voltage that can be supplied by the output pin.
It is limited by the output stage transistor and generally less than V_{CC}.
d. Output Current Rating (Io)
Maximum current that can be furnished by the output stage. It is limited by the rating of the output transistor.
e. Input Forward Current Rating (I_F)
Maximum current that can flow from the input pin. It is generally a function of the input voltage rating.
f. Input Reverse Current Rating (I_R)
Maximum current that can flow to the input pin.
g. Maximum Power Rating (Pd max)
Maximum consumed power that can be permitted in the IC. It is generally dependant on processing and package type.
h. Operating Temperature Rating (Topr)
It is the temperature range that can be operated over to be within spec. limits. Generally, for industrial and commercial applications, it is specified as follows:
Industrial: $-55°C \sim +125°C$ (Specially $-65°C \sim +150°C$)
Commercial: $0°C \sim +70°C$
i. Maximum Storage Temperature Rating (Tstg)
This is limited by the package material, along with the intrinsic characteristics of a particular semiconductor.

3.2 Derating

Semiconductor reliability is a function of electrical, thermal, and mechanical stressing. All of these must be considered in the design of a system. Within reason, the further the semiconductor device is operated below (derated) its maximum rating, the more reliable the device will be. Temperature is one of the main factors affecting the reliability of semiconductor devices. The failure rate increases rapidly with a rise in junction temperature, and follows the Arrhenius law:

$$\lambda = A\exp(-Ea/KT)$$

Where,
λ = failure rate
A = Constant
K = Boltzman's constant
Ea = Activation energy
Tj = Junction temperature

Taking a typical activation energy for random failures as 1 eV, this gives a six fold increase in failure rate for a temperature rise of 20°C In general, activatio energyis in the range 0.3~0.6 eV (typically 0.4 eV) for infant mortality failures, and 0.6~1.3 eV for rndom failures.
To maximize reliability, designers should keep the junction temperature as low as possible. For high and medium power dissipation devices, Samsung uses copper lead frames with a low thermal resistance to simplify this taks. In table VI, derating design standards that must be considered in reliability design are explained. In system design, it is advisable to adjust within derating levels. When it is impossible to adjust within derating levels, selecting a higher level device or some other alternative is necessary.

3.3 Derating Design Standard

Derating Factor		Diode	Transistor	IC	Remark
Temperature	Junction Temperature	Below 110°C ‡ (Below Tj=60°C)	S/S Below 150°C Power Below 150°C	Below 125°C	Ge: Below 65°C
	Ambient Temperature	Ta=0 – 45°C			
	Other	Power Dissipation, Thermal Condition: Tj=Pd×θ ja+Ta			
Humidity	Relative Humidity	RH=40 – 80%	RH=40 – 80%	RH=40 – 80%	
	Other	Generally, printed circuit board must be coated to protect against moisture, which forms due to a sudden drop in temperature			
Voltage	Endurance Voltage	Below V_{CC}(max) × 0.8 ‡ V_{CC}(max) × 0.5		According to Catalog Spec.	
	Overload Voltage	If electrostatic destrution is assumed, supply voltage must be protected against overload			
Current	Average Current	Below Ic(max) × 0.5 ‡ Below Ic(max) × 0.25	Below Ic(peak) × 0.8	Below Ic(max) × 0.5 (Especially Power Ic)	
	Peak Current	Below Ic(peak) × 0.8	Below Ic(peak) × 0.8	Below Ic(peak) × 0.8	
Power	Average Power	Below Pd(max) × 0.5 (Especially Zener Diode)	Below Pd(max) × 0.5 (Especially Power Transistor)	Below Pd(max) × 0.5 (Especially Power Application)	
Pulse	SOA	Do not exceed maximum rating			
	Surge	Below I_F(Surge)	Below Ic(peak)	Below Ic(Peak)	

Note: 1. Exclude special use condition
2. ‡ All derating factors must be satisfied simultaneously for high reliability application
3. SOA represents Safe Operating Area

Table VI. Semiconductor Derating Table

3.4 Electrostic Discharge Protection

Electronic components need to be protected from the hazards of static electricity; from the manufacturing stage to where they are utilized. MOS devices can be damaged by ESD due to improper handling or installation. The thin oxide layers can be destroyed by an electric field.

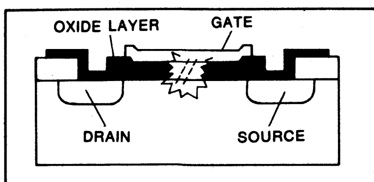

Fig 25. ESD failure

A. Handle all components at a static safeguarded work area.
B. Transport all components in static shielding containers or packages.
C. Education of all personnel in proper handling of components.

To comply with these rules, the following procedures must be set up:
1) Wear static control wrist straps (from a qualified source), and use properly.
2) Each table top must be protected with a conductive mat, properly grounded.
3) Extended use of conductive floor mats.
4) Static control shoe straps, where people typically wear insulative footwear (i.e. shoes with crepe or thick rubber soles).
5) Ionized air blowers are a necessary part of the protective system, to neutralize static charge on conductive items.
6) Use only grounded-tip type soldering irons
7) Single components, tubes, and printed circuit boards should always be contained in static shielding bags. Parts should be kept in the original bags up to the very last point in a user's production line.
8) If bigger containers (Tote Box) are used for in-plant transport of devices on PC boards, they must be electrically conductive, like the carbon loaded variety.
9) All tools, persons and testing machines, which could contact device leads, must be conductive and grounded.
10) Avoid the use of high dielectric materials (like polystyrene) for subassembly, construction, storing, and transportion.
11) Follow a proper power supply sequence for testing and application. Supply voltages should be applied before and removed after input signals. Insertion and removal from sockets should be done with no power applied.
12) Fitration, noise suppression, and slow voltage surges should be guaranteed on the supply lines.